A Dual UPQC to Mitigate Sag/Swell, Interruption, and Harmonics on Three Phase Low Voltage Distribution System

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Abstract-The Unified Power Quality Conditioner (UPQC) is a combination of a series active filter (SeAF) and a shunt active filter (ShAF) connected in parallel by a DC link capacitor. This device can mitigate power quality (PQ) problems i.e. sag/swell, harmonics, and unbalance on the source and load bus of three-phase three-wire (3P3W) on low voltage distribution systems simultaneously. The disadvantage of UPQC is that it is unable to overcome the voltage interruption so that the source can not deliver power to the load. This paper proposes a dual UPQC model to overcome the voltage interruption on the source bus so that the load bus continues to get power supply. There are six disturbance cases i.e. sinusoidal supply-sag-non-linear load (S-Sag-NL-L), sinusoidal supply-swell-NL-L (S-Swell-NL-L), sinusoidal-interruption-NL-L (S-Inter-NL-L), distorted supply-sag-NL-L load (D-Sag-NL-L), distorted supply-swell-NL-L (D-Swell-NL-L), and distorted supply-interruption-NL-LL (D-Inter-NL-L). The proportional Integral (PI) method is used to control the SeAF and the ShAF in the dual UPQC circuit model. The simulation results show that in the D-Inter-NL-LL case, a Dual UPQC model can maintain a load voltage magnitude of 266.60 V (voltage drop only of 14%), higher compared to a Single UPQC model of 173.97 V (voltage drop of 43.88%). In the same case, a dual UPQC model is capable of resulting in an average total harmonics distortion (THD) of load voltage of 10.10%, lower compared to a single UPQC model of 26.70%.

Keywords—Dual/Single UPQC, Sag/Swell, Interruption, Harmonics.

I. Introduction

In recent decades, the use of NL-Ls by customers has contributed to a decrease in the PQ in power system, causing current distortion in the load buses. On the other hand, the presence of sensitive loads and voltage distortion on the source bus also causes several voltage disturbances, thereby also causing a decrease in voltage. To solve the problem of worsening PQ due to the use of sensitive loads/NL-Ls and voltage distortion, a single UPQC is proposed [1]. The single UPQC consists of a SeAF and a ShAF connected in parallel via a DC-link capacitor and serves to mitigate a number of PQ problems on the source and load sides simultaneously [2]. The SeAF functions to reduce several of voltage disturbances on the source bus. Meanwhile, the ShAF functions to overcome several current quality problems on the load bus [3].

To anticipate the failure of both inverters in a single UPQC circuit, a dual UPQC model was developed. The advantage of a dual UPQC is that it has a more reliable inverter circuit structure and control because if there is a disturbance in one of the inverters, the UPQC system is still able to operate normally [4]. The dual or interline UPQC consists of two active filters, namely SeAF and ShAF (parallel active filters). Different from the single UPQC, the dual UPQC has a SeAF which is controlled as a sinusoidal current source, and a ShAF which is controlled as a sinusoidal voltage source. Thus the dual UPQC with pulse width modulation (PWM) control is controlled using a sinusoidal reference, in contrast to a single UPQC which is still controlled using a non-sinusoidal reference.

Implementation of dual UPQC circuit and control, to improve PQ on the source and load side of the low voltage distribution system has been discussed in several papers. The simplification technique UPQC control has been proposed in [5] and developed on the ABC reference frame using the sinusoidal reference synchronization theory. In [6], a comparison of two different controls has been carried out to generate the PWM reference signal using the α-β and d-q reference frames, respectively. The comparison of the operating performance of single UPQC and dual UPQC in a 3 phase 3 wire (3P3W) system under static and dynamic disturbances has been carried out through simulations [7] and experiments [8]. The improvement of PQ using dual UPQC under conditions of sudden load changes has been done by [9]. The study, analysis, and implementation of the dual UPQC model that can be connected to a 3P3W or three-phase four-wire (3P4W) [10] and 3P4W distribution system [11] with PI control have been applied. The analysis to balance reactive power between SeAF and ShAF on a dual UPQC using power angle control has been carried out in [12]. The weakness of the UPQC is that it is unable to overcome the disturbance caused by interruption voltage on the source bus so that the load bus experiences blackouts [3].

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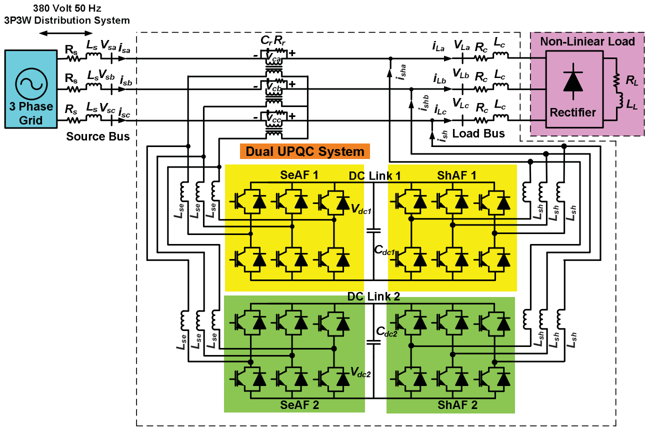

Fig. 1 Proposed model of a dual UPQC connected to 3P3W system

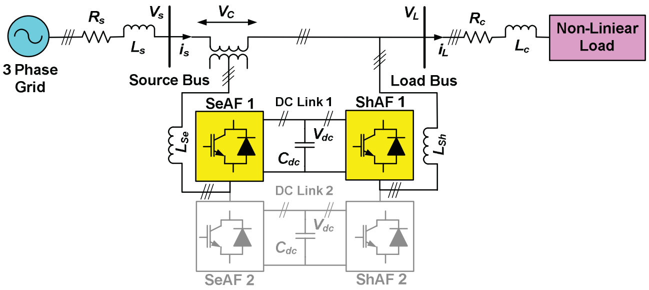

Fig. 2. Model of a single UPQC in single phase system

The paper proposes a dual UPQC model to overcome interruption voltage in the source bus so that the load bus still gets power supply. To provide a performance of the proposed model, the simulation parameter results of the dual UPQC model are further validated with a single UPQC model.

II. RESEARCH METHOD

A. Proposed Method

This research aims to mitigate interruption voltage, sag/swell voltage, and harmonics in the 3P3W distribution system using a dual UPQC model. This power electronic device is used to overcome the weakness of a single UPQC in maintaining the magnitude of load voltage so that the load bus is still supplied with power if interruption voltage happens on the source bus. The dual UPQC circuit is located between the load bus and connected to the source bus (PCC) via a 380 V (L-L) low-voltage distribution line with a frequency of 50 Hz. The PI controller is used in a dual UPQC circuit model. There are six disturbance cases i.e. (1) S-Swell-NL-L, (2) S-Sag-NL-L, (3) S-Inter-NL-L, (4) D-Swell-NL-L, (5) D-Sag-NL-L, and (6) D-Inter-NL-L.

In case 1, the system is connected to a NL-L and the sinusoidal source runs into a swell voltage of 50%. In case 2, the system is connected to a NL-L and the sinusoidal source runs into a sag voltage of 50%. In case 3, the system is connected to a NL-L and the sinusoidal source runs into an interruption voltage of 100%. In case 4, the system is connected to a NL-L, the source generates 5^{th} and 7^{th} odd-order harmonic components with individual harmonic distortion each of 5% and 2%, as well as runs into a swell voltage of 50%. In case 5, the system is connected to a NL-L, the source generates 5^{th} and 7^{th} odd-order harmonic components with individual harmonic distortion values each of 5% and 2%, as well as runs into a sag voltage of 50%. In case 6, the system is connected to a NL-L, the source generates 5^{th} and 7^{th} odd-order harmonic components with individual harmonic distortion each of 5% and 2%, as well as runs into interruption voltage of 100%. The total simulation time for all disturbance cases is equal to 0.7 s with a disturbance duration of 0.3 s between t = 0.2 s to t = 0.5 s.

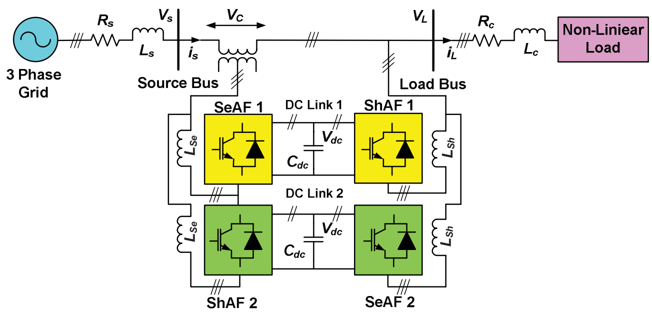

Fig. 3. Model of a dual UPQC in single phase system.

The mitigation analysis of PQ problems in this paper i.e. improve load voltage magnitude and reduce harmonics due to interruption voltage, sag/swell voltage, and source voltage harmonic distortion, as well as reduce source current harmonics due to NL-Ls. Finally, the simulation results of all parameters in a dual UPQC model are then validated with a single UPQC model to provide an overview of the performance advantages of the proposed model. Figure 1 shows the proposed model of a dual UPQC connected to a 3P3W distribution system. Figure 2 and Figure 3 show the proposed model of a single and a dual UPQC in a single-phase system. The parameter of the proposed model is shown in Appendix I.

B. Control of Dual Series Active Filter

The SeAF control on a single UPQC has been fully described in [13]. Based on this circuit model, the SeAF control circuit on the dual UPQC is arranged by duplicating a single SeAF control circuit while still using one series of three-phase series transformers. Then based on this procedure, the authors further propose complete control of the dual UPQC whose model is shown in Figure 4. The distorted source voltage is calculated and divided by the base input voltage peak amplitude V_m , as described in Eq. (1) [14].

$$V_m = \sqrt{\frac{2}{3}(V_{sa}^2 + V_{sb}^2 + V_{sc}^2)} \quad (1)$$

C, Control of Dual Shunt Active Filter

The ShAF control on a single UPQC has been described in detail in [13]. Based on this circuit model, the dual UPQC ShAF control circuit is arranged by duplicating the control circuit on a single ShAF. Using the "p-q" method, the voltages and currents can be transformed into the $\alpha - \beta$. The axis as indicated in Eq. (2) and Eq. (3) [15].

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (2)$$

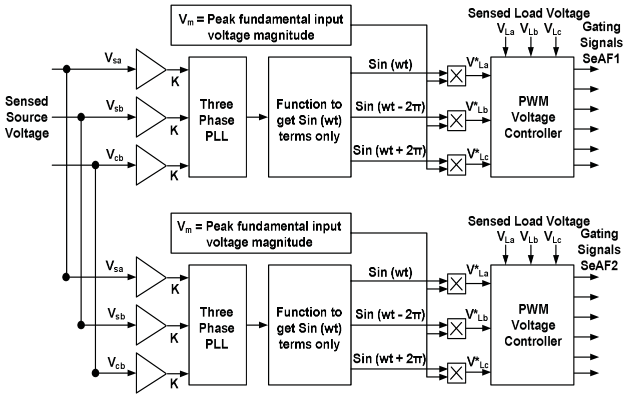

Fig. 4 Dual series active filter control

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (3)$$

The computation of true power (p) and imaginary power (q) is presented in Eq. (4)[14].

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (4)$$

$$p = \bar{p} + \tilde{p} \ ; \ q = \bar{q} + \tilde{q} \quad (5)$$

The total imaginary power (q) and fluctuating component of true power $(\tilde{p})$ are chosen as power references and current references and are used by using Eq. (5) to balance the harmonics and reactive power [16].

$$\begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} -\tilde{p} + \bar{p}_{loss} \\ -q \end{bmatrix} \quad (6)$$

The authors propose a model of a dual ShAF control presented in Figure 5.

The $\bar{p}_{loss}$ parameter is collected from the voltage controller and is used as average true power. The compensation current $(i_{c\alpha}^*, i_{c\beta}^*)$ is used to fulfill load power consumption as presented in Eq. (6). The current is stated in coordinates $\alpha - \beta$. The current compensation is needed to gain source current in each phase by using Eq. (7). The source current in each phase $(i_{sa}^*, i_{sa}^*, i_{sa}^*)$ is stated in the ABC coordinates gained from the compensation current in $\alpha\beta$ axis and is expressed in Eq. 7 [16].

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \end{bmatrix} \quad (7)$$

To operate properly, the dual UPQC must have a minimum DC-link voltage(V_{dc}) stated in Eq.8 [17]:

$$V_{dc} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}m} \quad (8)$$

Using the modulation value (m) equal to 1 and the line to line source voltage (V_{LL}) of 380 V, V_{dc} was calculated to be equal to 620.54 V and set at 650 V. The dual ShAF input indicated in Fig. 6 is DC voltage 1 (V_{dc1}) and reference of DC

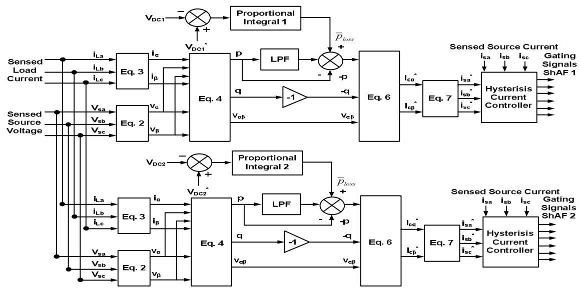

Fig. 5. Dual shunt active filter control

voltage 1 (V_{dc1}^*) as well as DC voltage 2 (V_{dc2}) and reference of DC voltage 2 (V_{dc2}^*), while P_{loss} is selected as the output using the PI controllers 1 and 2. Furthermore, P_{loss} will be an input variable to generate the reference source currents $(i_{sa}^*, i_{sa}^*, i_{sa}^*)$. Then, the reference source currents output is compared with the current sources (i_{sa}, i_{sb}, i_{sc}) by hysteresis current regulator to result in a trigger signal in the IGBT circuit of ShAF 1 and ShAF 2. In this paper, the PI controllers 1 and 2 are proposed as the control algorithms of the DC voltages 1 and 2 on ShAF 1 and ShAF 2, respectively.

D. Percentage of Sag/Swell and Interruption Voltage

The standard of monitoring sag/swell and interruption voltage as a part of PQ parameters is IEEE 1159-1995 [18]. This standard presents a definition and table of voltage sag/voltage and interruption base on categories (instantaneous, momentary, and temporary) typical duration, and typical magnitude. The percentage of disturbances i.e. sag/swell and interruption voltage are proposed by authors in Eq. (9) below:

$$Disturb\ Voltage\ (\%) = \frac{|Vpre\_disturb - V\_disturb|}{Vpre\_disturb} \quad (9)$$

II. RESULT AND DISCUSSION

The proposed model analysis is carried out by set two UPQC models, i.e. single UPQC and dual UPQC. There are six disturbance cases in each UPQC i.e. (1) S-Swell-NL-L, (2) S-Sag-NL-L, (3) S-Inter-NL-L, (4) D-Swell-NL-L, (5) D-Sag-NL-L, and (6) D-Inter-NL-L. Using Matlab/Simulink, the model is run based on selected cases to get the magnitude of source voltages (V_{Sa}, V_{Sa}, V_{Sa}), load voltages (V_{La}, V_{Lb}, V_{Lc}), source currents (I_{Sa}, I_{Sb}, I_{Sc}), and load currents (I_{La}, I_{Lb}, I_{Lc}) as well as their average values. Furthermore, THD of source voltage, THD of load voltage THD of source current, and THD of load current in each phase, and their average value are also determined based on the curves obtained previously. The total simulation period lasts 0.7 s with a duration of disturbance between 0.2-0.5 s. The THD of voltage and current in each phase is determined in one cycle starting at t = 0.35 s. Based on the load voltage value, then disturbance voltage percentage value (%) is obtained using equation (9), with a pre-disturbance voltage of 310 V. The simulation results of voltage and current magnitudes, THD of voltage and current, and percentage of load voltage disturbances in six cases are presented in Table 1, Table 2, (Appendix II) and Table 3 respectively. Figure 6 and Figure 7 (Appendix III) show the performance of a single UPQC and a dual UPQC respectively, in the D-Inter-NL-L case.

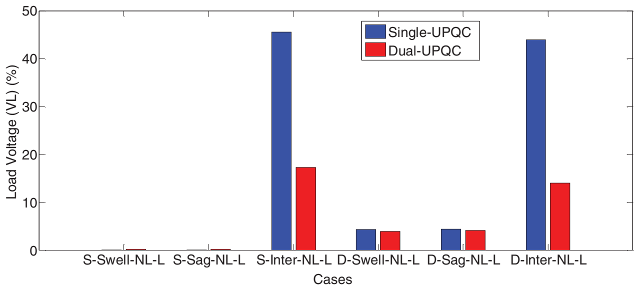

Fig. 8. Performance of the load voltage percentage between a Single-UPQC and a Dual-UPQC

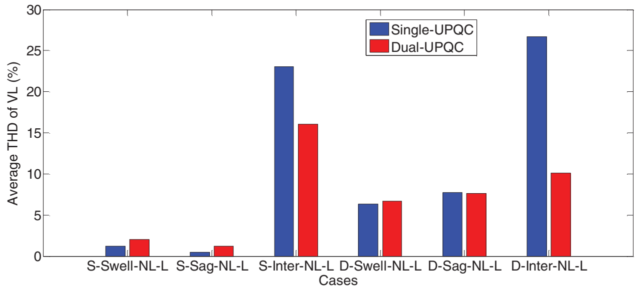

Fig. 9. Performance of the average load voltage harmonics between a Single -UPQC and a Dual-U

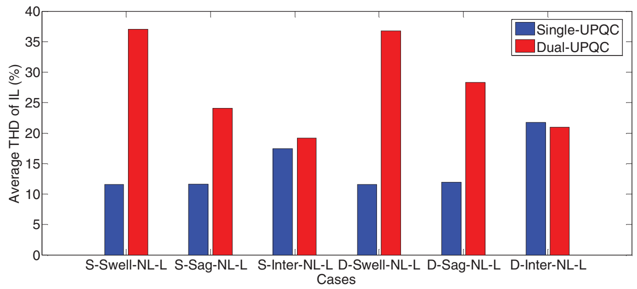

Fig. 10. Performance of the average source current harmonics between a Single-UPQC and a Dual-UPQC

Table 1 and Figure 8 show that in both S-Sag/Swell-NL-L and D-Sag/Swell-NL-L cases, the implementation of a dual UPQC model results in a slightly higher percentage of load voltage disturbance than a single UPQC model. In the D-Inter-NL-L case, a dual UPQC model is able to maintain a more stable load voltage of 266.60 V compared to a single UPQC model of 173.97 V. Table 3 and Figure 8 also show that in the D-Inter-NL-L case, a dual UPQC circuit is also capable of resulting in a smaller percentage of load voltage disturbance of 14%, compared to a single UPQC circuit of 43.88%. In this case, the SeAF circuit on a Dual UPQC with PI controller can inject a larger series power, so that it is also able to produce a higher load voltage and a lower percentage of load voltage disturbance than a single UPQC.

Table 2 and Figure 9 show that in both S-Sag/Swell-NL-L and D-Sag/Swell-NL-L fault cases, the implementation of a dual UPQC model results in a slightly higher average THD of the load voltage than a single UPQC model. In the D-Inter-NL-LL case, a dual UPQC circuit can produce a much lower load voltage average THD of 10.10% compared to a single UPQC circuit of 26.70 %. In this case, the SeAF circuit on a dual UPQC with PI controller can inject a larger series compensation voltage, so that it is also able to reduce the harmonics content of load voltage and result in the average THD value is smaller than a single UPQC.

Table 2 and Figure 10 show that in S-Sag/Swell-NL-L and D-Sag/Swell-NL-L cases, the implementation of a dual UPQC model produces higher source current average THD than a single UPQC model. In the D-Inter-NL-L case, a dual UPQC circuit can produce a slightly lower source current average THD of 21.01% compared to a single UPQC circuit of 21.77%. In this case, the ShAF circuit on a dual UPQC with PI controller is able to inject a slightly larger shunt compensation current, so that it is also able to reduce the harmonics content of source current, and result in the average THD value is slightly smaller than a single UPQC.

IV. Conclusion

The implementation of UPQC to mitigate PQ problems i.e. sag/swell, interruption, and harmonics on the source and load bus of 3P3W on low voltage distribution system simultaneously has been presented. There are six disturbance cases i.e. S-Sag-NL-L, S-Swell-NL-L, S-Inter-NL-L, D-Sag-NL-L, D-Swell-NL-L, and D-Inter-NL-L. The PI method is used to control SeAF and ShAF in the dual UPQC circuit model. The simulation results show that in the D-Inter-NL-L case, a dual UPQC model is able to maintain a load voltage magnitude, higher compared to a single UPQC model. In the D-Inter-NL-L case, a dual UPQC circuit is also capable of resulting in a smaller percentage of load voltage disturbance compared to a single UPQC circuit. In the same case, a dual UPQC model is capable of resulting in an average THD of load voltage, lower compared to a single UPQC model. In the D-Inter-NL-L case, the percentage of load voltage disturbance on a 3P3W system using a dual UPQC still has not reached the limit below 10 percent. The THD of load voltage and source current also still exceed the IEEE-519 standard. The implementation of renewable energy generators i.e. a photovoltaic and/or a wind turbine as well as advanced control based on artificial intelligence on ShAF circuits i.e. fuzzy logic, neural network, or ANFIS, then can be selected as future work to overcome this problem.

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APPENDIX I

The 3P3W source: root means square voltage 380 V (line to line), 50 Hz, line impedance: R_S = 0.1 ohm, L_S = 15 mH; SeAF and ShAF: series inductance L_{Se} = 0.015 mH; shunt inductance L_{Sh} = 15 mH; compensation transformer: rating 10 kVA, 50 Hz, transformation ratio (N_1/N_2) = 1:1; NL-L: resistance R_L = 60 ohm, inductance L_L = 0.15 mH, load impedance R_C = 0.4 ohm and L_C = 15 mH; DC-link 1 and 2: DC voltage 1 and 2 V_{dc} = 650 volt and capacitance 1 and 2 C_{dc} = 3000 μF; PI controller 1 and 2: K_P = 0.2, K_I= 1.5; input: $V_{dc-error}$ and $\Delta V_{dc-error}$; output: power losses ($\bar{p}_{loss}$).

APPENDIX II

TABLE I. MAGNITUDE OF VOLTAGE AND CURRENT USING SINGLE UPQC AND DUAL UPQC ON SIX DISTURBANCE CASES

Case	Source Voltage V_S (V)				Load Voltage V_L (V)				Source Current I_S (A)				Load Current I_L (A)			
	A	*B*	*C*	*Avg*	*A*	*B*	*C*	*Avg*	*A*	*B*	*C*	*Avg*	*A*	*B*	*C*	*Avg*
Single UPQC																
1	464.4	464.6	464.6	**464.53**	310.0	309.9	309.9	**309.93**	8.381	8.382	8.379	**8.381**	8.586	8.584	8.585	**8.585**
2	153.4	153.4	153.4	**153.40**	310.1	310.1	310.1	**310.10**	16.61	16.38	16.42	**16.470**	8.588	8.586	8.589	**8.588**
3	0.9984	0.8963	1.022	**0.970**	172.2	161.5	173.3	**169.00**	9.345	8.621	9.130	**9.032**	4.647	4.356	4.606	**4.536**
4	464.6	464.6	464.6	**464.60**	320.2	322.8	326.9	**323.30**	8.732	8.697	8.723	**8.717**	8.927	8.974	8.991	**8.964**
5	153.7	153.8	153.7	**153.73**	295.6	296.0	297.5	**296.37**	13.97	13.45	14.00	**13.807**	8.245	8.17	9.097	**8.504**
6	0.9641	1.136	0.8586	**0.990**	173.7	179.6	168.6	**173.97**	8.601	10.27	8.507	**9.126**	5.105	4.561	4.589	**4.752**
Dual UPQC																
1	464.8	464.8	464.8	**464.80**	310.4	310.4	310.5	**310.43**	10.45	10.46	10.44	**10.450**	8.605	8.604	8.604	**8.604**
2	154.1	154.1	154.1	**154.10**	309.4	309.5	309.4	**309.43**	13.84	13.9	13.92	**13.887**	8.567	8.557	8.574	**8.566**
3	1.728	1.634	1.868	**1.74**	256.5	245	268.1	**256.53**	16.61	15.42	19.94	**17.323**	7.323	6.8	7.192	**7.105**
4	464.8	464.8	464.8	**464.80**	318.9	321.9	325.9	**322.23**	10.97	10.86	10.92	**10.917**	8.916	8.934	8.934	**8.928**
5	154.3	154.3	154.2	**154.27**	297.3	299	295.6	**297.30**	12.12	12.68	12.68	**12.493**	8.286	8.342	8.098	**8.242**
6	1.404	1.473	1.621	**1.50**	266.4	267.1	266.3	**266.60**	12.66	13.27	16.71	**14.213**	7.018	7.441	7.365	**7.275**

TABLE II. THD OF VOLTAGE AND CURRENT USING SINGLE UPQC AND DUAL UPQC ON SIX DISTURBANCE CASES

Case	Source Voltage THD (%)				Load Voltage THD (%)				Source Current THD (%)				Load Current THD (%)			
	A	*B*	*C*	*Avg*	*A*	*B*	*C*	*Avg*	*A*	*B*	*C*	*Avg*	*A*	*B*	*C*	*Avg*
Single UPQC																
1	0.79	0.78	0.79	**0.79**	1.24	1.23	1.24	**1.24**	11.63	11.57	11.57	**11.59**	22.30	22.30	22.30	**22.30**
2	0.98	0,98	0.98	**0.65**	0.49	0.49	0.48	**0.49**	11.68	11.68	11.59	**11.65**	22.28	22.29	22.28	**22.28**
3	83.18	109.82	87.01	**93.34**	23.84	24.37	21.02	**23.08**	20.66	19.45	12.23	**17.45**	26.84	21.48	17.66	**21.99**
4	3.63	3.67	3.71	**3.67**	4.90	6.42	7.69	**6.34**	11.63	11.42	11.71	**11.59**	22.46	21.82	22.47	**22.25**
5	11.07	10.9	10.76	**10.91**	8.41	7.80	7.09	**7.77**	11.14	12.93	11.76	**11.94**	21.76	23.42	21.77	**22.32**
6	1756.97	1463	1917	**1712.32**	21.53	31.74	26.82	**26.70**	17.16	21.84	26.31	**21.77**	24.96	31.51	24.62	**27.03**
Dual UPQC																
1	1.35	1.36	1.36	**1.36**	2.06	2.08	2.07	**2.07**	36.9	36.91	37.09	**36.97**	22.36	22.35	22.37	**22.36**
2	2.47	2.44	2.49	**2.47**	1.24	1.22	1.26	**1.24**	24.07	23.98	24.14	**24.06**	22.36	22.35	22.38	**22.36**
3	147.28	154.6	132.19	**144.69**	16.53	13.1	18.56	**16.06**	21.00	16.69	19.94	**19.21**	24.30	22.91	22.82	**23.34**
4	3.68	3.82	3.98	**3.83**	5.36	6.55	8.16	**6.69**	36.71	36.46	37.11	**36.76**	22.40	22.17	22.54	**22.37**
5	10.87	10.97	11.64	**11.16**	6.92	7.12	8.86	**7.63**	28.85	26.10	29.88	**28.28**	22.15	23.19	23.14	**22.83**
6	1211.59	1139.13	1053.34	**1134.69**	11.21	11.64	7.45	**10.10**	24.82	21.50	16.71	**21.01**	22.07	22.65	22.13	**22.28**

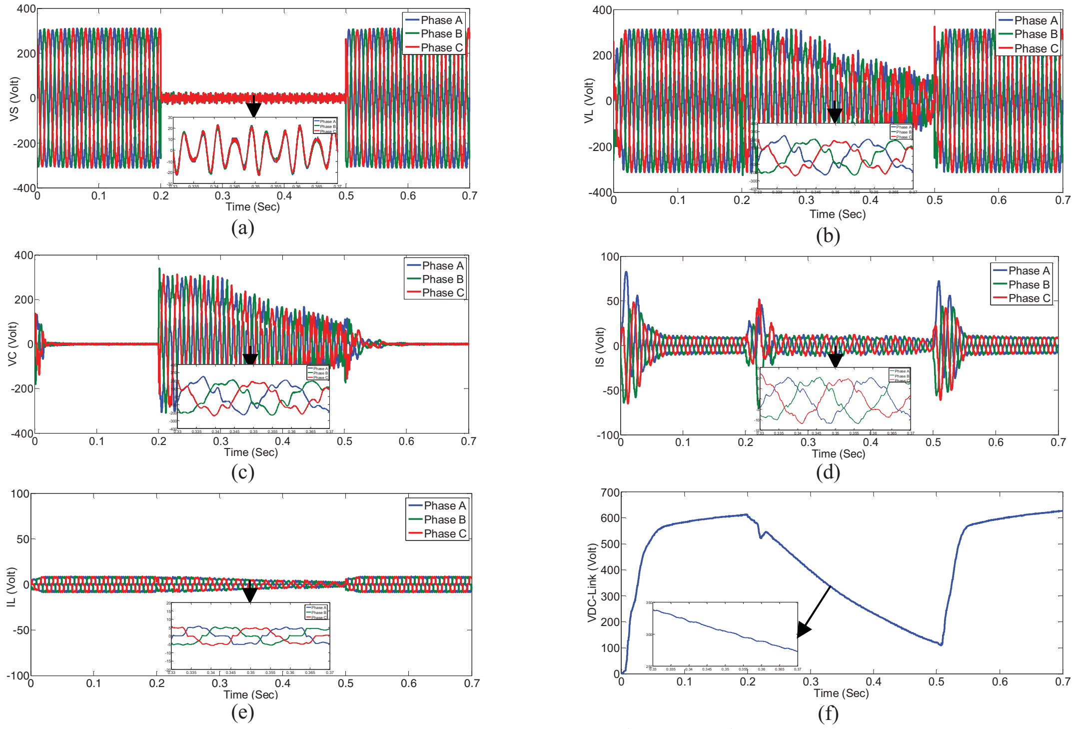

Fig. 6. Performance of a single UPQC under Dis-Inter-NL-L case: (a) source voltages (V_{Sa}, V_{Sa}, V_{Sa}); (b) load voltages (V_{La}, V_{Lb}, V_{Lc}); (c) compensation voltages (V_{Ca}, V_{Cb}, V_{Cc}); (c) source currents (I_{Sa}, I_{Sb}, I_{Sc}); load currents (I_{La}, I_{Lb}, I_{Lc}); and DC-link voltage $(V_{DC-Link})$

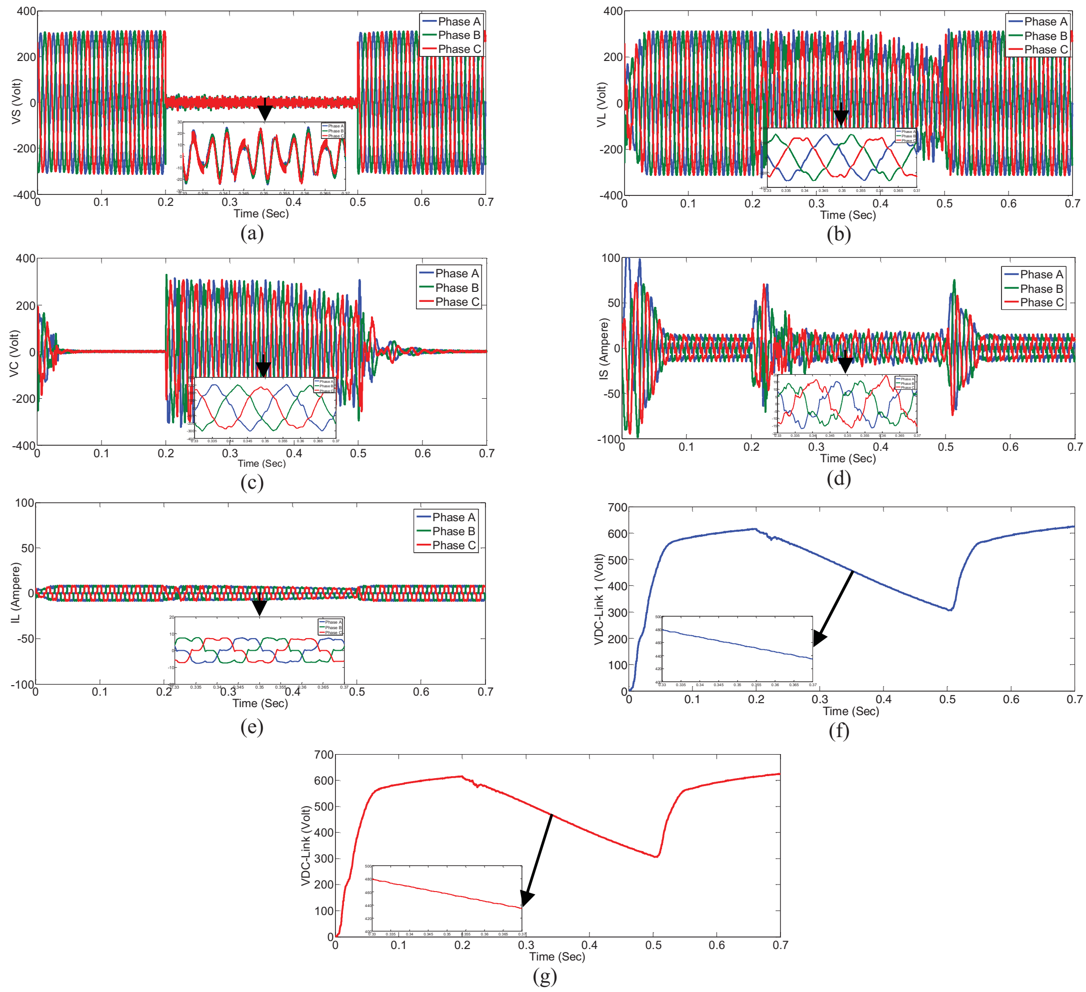

Fig. 7. Performance of a dual UPQC under Dis-Inter-NL-L case: (a) source voltages (V_{Sa}, V_{Sa}, V_{Sa}); (b) load voltages (V_{La}, V_{Lb}, V_{Lc}); (c) compensation voltages (V_{Ca}, V_{Cb}, V_{Cc}); (d) source currents (I_{Sa}, I_{Sb}, I_{Sc}); (e) load currents (I_{La}, I_{Lb}, I_{Lc}); (f) DC-link voltage 1 $(V_{DC-Link1})$; and (g) DC-link voltage 2 $(V_{DC-Link2})$