YAYASAN BRATA BHAKTI DAERAH JAWA TIMUR
UNIVERSITAS BHAYANGKARA SURABAYA
LEMBAGA PENELITIAN DAN PENGABDIAN PADA MASYARAKAT
(LPPM)
Kampus : Jl. A. Yani 114 Surabaya Telp. 031 - 8285602, 8291055, Fax. 031 - 8285601

SURAT KETERANGAN

Nomor: Sket/ 7 /I/2023/LPPM/UBHARA

Kepala Lembaga Penelitian dan Pengabdian kepada Masyarakat (LPPM) Universitas Bhayangkara Surabaya menerangkan bahwa:

Nama : Dr. Amirullah, ST, MT.
NIP : 197705202005011001
NIDN : 0020057701
Unit Kerja : Universitas Bhayangkara Surabaya

Benar telah melakukan kegiatan:

1. Menulis jurnal berjudul Implementation of Single-Phase DVR-BES Based on Unit Vector Template Generation (UVTG) to Mitigate Voltage Sag Using Arduino Uno and Monitored in Real-Time Through LabVIEW Simulation (Yohanes Artha Setiawan dan Amirullah Amirullah) yang telah dipublikasikan di International Journal of Intelligent Engineering and Systems (IJIES), Vol.14, No.3, 2021, pp. 82-96, ISSN: 2185-3118, Publisher: The Intilligent Network and Systems Society, **Terindeks Scopus Q2.**
2. Telah melakukan korespondensi melalui email dalam proses penerbitan jurnal tersebut. Bukti korespondensi email dan bukti pendukung adalah benar sudah dilakukan oleh yang bersangkutan serta sudah dilampirkan bersama surat ini.

Demikian surat keterangan ini dibuat untuk kepentingan kelengkapan pengusulan Guru Besar.

Surabaya, 20 Januari 2023
Kepala LPPM

Drs. Heru Irianto, M.Si.
NIP. 9000028

Lampiran 1

Bukti Korespondensi Email dengan Editor/Pengelola Jurnal

Ubhara Surabaya

Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Send Paper Amirullah Ubhara Surabaya Indonesia

1 pesan

Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id> 24 November 2020 pukul 15.47
Kepada: ijies@inass.org
Cc: ijies@inass.org
Bcc: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Dear Prof. Kei Eguchi,

I send you the paper entitled **Implementation of Single-Phase DVR-BES Based on Unit Vector Template Generation (UVTG) to Mitigate Voltage Sag Using Arduino Uno and Monitored in Real-Time Through LabVIEW Simulation to IJIES (INASS Publisher).**

I also attached the manuscript and cover letter to this email.

This is my email and thanks for your cooperation.

Dr. Amirullah
Universitas Bhayangkara Surabaya
Surabaya Indonesia

2 lampiran

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Ubhara Surabaya

Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

ijies3819: Send Paper Amirullah Ubhara Surabaya Indonesia

10 pesan

EGUCHI Kei <eguti@fit.ac.jp> 24 November 2020 pukul 16.10
Kepada: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Dear author(s),

Thank you for your interest and support to IJIES.
I am hereby to confirm the delivery of your paper, Paper ID is " ijies3819".
It has been sent for reviewing.
The notification will be feedback within one month.
Appreciate your patiently wait.

If you have any question, please contact us with your paper ID.

Best regards,
IJIES Editors

From: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>
Sent: Tuesday, November 24, 2020 5:48 PM
To: ijies@inass.org
Subject: Send Paper Amirullah Ubhara Surabaya Indonesia

Dear Prof. Kei Eguchi,

I send you the paper entitled Implementation of Single-Phase DVR-BES Based on Unit Vector Template Generation (UVTG) to Mitigate Voltage Sag Using Arduino Uno and Monitored in Real-Time Through LabVIEW Simulation to IJIES (INASS Publisher).

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Dr. Amirullah
Universitas Bhayangkara Surabaya
Surabaya Indonesia

Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id> 24 November 2020 pukul 17.45
Kepada: EGUCHI Kei <eguti@fit.ac.jp>
Cc: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>
Bcc: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Dear IJIES Editor,

Thanks a lot for your response.

Dr. Amirullah
Universitas Bhayangkara Surabaya
Surabaya East-Java Indonesia

[Kutipan teks disembunyikan]

EGUCHI Kei <eguti@fit.ac.jp> 9 Desember 2020 pukul 13.39
Kepada: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Dear author(s),

Congratulations!
The 1st review for your paper was accepted.
However, we are sorry to inform you that your paper cannot be recommended for publication in IJIES, in its current form.
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Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id> 10 Desember 2020 pukul 05.00
Kepada: EGUCHI Kei <eguti@fit.ac.jp>
Cc: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>
Bcc: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Dear Prof. Kei Eguchi,

Thanks a lot for your information.

Dr. Amirullah
Universitas Bhayangkara Surabaya
Surabaya Indonesia
[Kutipan teks disembunyikan]

Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id> 17 Januari 2021 pukul 06.23
Kepada: EGUCHI Kei <eguti@fit.ac.jp>
Cc: Kei Eguchi <eguti@fit.ac.jp>
Bcc: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Dear Prof Kei Eguchi,

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差出人: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>
送信日時: 2021年1月17日 8:23
宛先: 江口 啓
件名: Re: ijies3819: Send Paper Amirullah Ubhara Surabaya Indonesia

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Surabaya-Indonesia

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Dr. Amirullah
Universitas Bhayangkara Surabaya
Surabaya Indonesia

[Kutipan teks disembunyikan]
[Kutipan teks disembunyikan]

EGUCHI Kei <eguti@fit.ac.jp> 17 Januari 2021 pukul 07.56

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Universitas Bhayangkara Surabaya
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[Kutipan teks disembunyikan]
[Kutipan teks disembunyikan]

Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id> 17 Januari 2021 pukul 08.43
Kepada: EGUCHI Kei <eguti@fit.ac.jp>
Cc: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>
Bcc: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Dear Prof. Kei Eguchi,

Thanks a lot for your response.

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Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id> 22 Januari 2021 pukul 10.25
Kepada: ijies@inass.org
Cc: Kei Eguchi <eguti@fit.ac.jp>
Bcc: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

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To: ijies@inass.org
Cc: 江口 啓 <eguti@fit.ac.jp>
Subject: Re: ijies3819: Send Paper Amirullah Ubhara Surabaya Indonesia

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Pada tanggal Kam, 10 Des 2020 pukul 05.00 Amirullah Ubhara Surabaya <mailto:amirullah@ubhara.ac.id <mailto:mailto:amirullah@ubhara.ac.id>> menulis:
Dear Prof. Kei Eguchi,

Thanks a lot for your information.

Dr. Amirullah
Universitas Bhayangkara Surabaya
Surabaya Indonesia

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From: Amirullah Ubhara Surabaya <mailto:amirullah@ubhara.ac.id<mailto:mailto:amirullah@ubhara.ac.id>>
Sent: Tuesday, November 24, 2020 5:48 PM
To: mailto:ijies@inass.org<mailto:mailto:ijies@inass.org>
Subject: Send Paper Amirullah Ubhara Surabaya Indonesia

Dear Prof. Kei Eguchi,

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I also attached the manuscript and cover letter to this email.

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Kepada: Kei Eguchi <eguti@fit.ac.jp>
Cc: ijies@inass.org
Bcc: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

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EGUCHI Kei <eguti@fit.ac.jp> 25 Januari 2021 pukul 16.16
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Paper ID: ijies3819

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Cc: 江口 啓 <eguti@fit.ac.jp>
Subject: Re: ijies3819: Send Paper Amirullah Ubhara Surabaya Indonesia

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Surabaya Indonesia

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2. Figure 5. ".....(D) load voltage (Vinj)" is revised to ".....(D) load voltage (VL)". (Page 89-pdf and marked in red font-doc).
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Received: October 18, 2020. Revised: December 20, 2020.

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Implementation of Single-Phase DVR-BES Based on Unit Vector Template Generation (UVTG) to Mitigate Voltage Sag Using Arduino Uno and Monitored in Real-Time Through LabVIEW Simulation

Yohanes Artha Setiawan[1] **Amirullah Amirullah**[1*]

[1]*Electrical Engineering Study Program, Faculty of Engineering, Universitas Bhayangkara Surabaya, Surabaya 60231, Indonesia*
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Abstract: This paper aims to design and implement a single-phase dynamic voltage restorer (DVR) supplied by battery energy storage (BES) using load voltage controlled by the unit vector template generation (UVTG) method. The UVTG method on the DVR system is implemented using the Arduino-Uno hardware. LabVIEW-based interface simulation is used for monitoring the parameter in real-time during 80% voltage sag period i.e. source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power factor measurements are also carried out to obtain total harmonic distortion (THD) of the source current and load current. The single-phase DVR system is connected to load i.e. a 5-watt bulb lamp (linear-load), 5-watt fluorescent (FL) lamp (non-linear load), and 5-watt light-emitting diode (LED) lamp (non-linear load). During voltage sag, the single-phase DVR-BES system is able to maintain load voltage i.e. bulb lamp, FL lamp, and LED lamp of 216 volts, 256 volts, and 185 volts, respectively. The percentage of load voltage disturbance at voltage sag for each load is 6.4%, 26.13%, and 8.87%, respectively. The measurement of source power-factor with voltage sag results in source true power factor of three loads of 0.985 leading, 0.985 leading, and 0.990 leading respectively. On the same system with voltage sag, single phase DVR-BES is able to result in source THD for three loads of 1.523%, 1.523%, and 1.010% respectively. Then for the system with 80% voltage sag and three types of loads, the LHE lamp is able to result in the best performance because it is able to produce the highest source current power factor and the lowest source current THD. The THD value of source current during voltage sag also had met the IEEE 519.

Keywords: Single Phase DVR, BES, Arduino Uno, LabVIEW, Voltage Sag

1. Introduction

During the last decade, there has been an increase in the number of sensitive and critical loads. On the other hand, the use of these tools also has an impact on deteriorating Power Quality (PQ). Among a number of PQ problems, problems related to voltage mitigation are also of increasing importance from a sensitive load and customer point of view. PQ problems related to voltage i.e. voltage sag, voltage swell, voltage harmonics, fluctuations, interruptions, and imbalance. In accordance with IEEE 1346 [1] and IEEE 1159 [2] standards, the sag voltage is defined as the RMS (root mean square) AC voltage sag with a magnitude of 10% to 90% of the nominal voltage, at power frequencies with a duration of 0.5 cycles to one minute. The voltage sag is caused by a single-phase short circuit to ground in the power system, starting in large-capacity induction motors, and sudden changes in the system connected to large loads [3]. Viewed from the system, the DVR is divided into two systems, namely one-phase DVR and three-phase DVR. Then three-phase DVR is connected to a 3 phase 3 wire (3P3W) or a 3 phase 4 wire (3P4W) system. Next, this paper will further focus on the design and implementation of single-phase DVRs to mitigate voltage sag at the source side and connect to a number of the linear/non-linear load. The simulation of low voltage single phase DVR based on the multilevel inverter to protect sensitive loads has been implemented

in [4]. The proposed model is able to compensate for the voltage sag and increase the PQ on the load side. A DVR topology using a cascaded multilevel direct pulse with modulation (PWM) ac-ac converter has been proposed in [5]. In this scheme, the unit cell of the multilevel converter consists of a single-phase ac-ac converter PWM using a switching cell (SC) structure that is paired with an inductor. The implementation of the phase shift PWM technique is capable of significantly reducing the size of the output filter inductor. One and three-phase DVR control schemes using PSCAD/EMTDC have been observed in [6]. The proposed system is able to compensate for a number of voltage sag variations and keep the load voltage constant. DVR control scheme with an ac-ac converter, based on voltage drop characterization has been investigated in [7] to reduce voltage drop with phase jumps. The superiority of the proposed control scheme is then validated on an ac-ac interphase converter topology. The vector-based one-phase DVR control using an improved synchronous reference frame (SRF) has been proposed in [8]. The vector analysis used in this control method during the voltage period was able to provide the magnitude and phase of the injection voltage.

The control methods to reduce sag voltages using a fuzzy logic controller (FLC) connected with sensitive loads [9] and distributed generation (DG) [10] have been proposed. The FLC control was used to generate pulses with the Sinusoidal Pulse Width Modulation (SPWM) technique at the output of an active filter circuit. Comparing to proportional-integral (PI) control, FLC control was able to provide better performance during voltage sag because it has more advantages in terms of resistance to parameter variations and system execution. A DVR with DG-connected FLC control also able to enhance voltage profiles, power quality, and reliability. Single-phase and three-phase DVRs use a single-phase ac to ac matrix converter to replace voltage source inverter (VSI), has been investigated by Matlab in [11],[12], and in PSCAD [13], at a number of variations in source voltage (sag, flicker, and unbalance). The single-phase DVR has been simulated in [14] and a special voltage detection method for single-phase DVRs has been introduced in [15]. The simulation results show that the DVR was able to maintain the nominal load voltage, despite interference and other abnormal conditions from the source side. The special detection method using double closed-loops of the proportional-resonant controller was also able to provide superior performance in voltage detection and compensation.

The DVR control scheme for reference voltage generation based on a single-phase Second Order Generalized Integrator-Phase Lock Lop (SOGI-PLL) using a series of active compensator has been observed in [16]. The proposed scheme is capable of dynamically responding, detecting, and rapidly compensating for sag/swell voltages without and with phase jumps. A DVR that uses a multilevel H-bridge inverter with a capacitor as an energy source has been introduced in [17]. This configuration allows the DVR to connect directly to a medium-voltage network, eliminating the need for a series injection transformer and batteries. The DVR model was the same but uses a single H-Bridge inverter and a battery on sag/swell voltage disturbances connected to the non-linear load which has also been observed in [18]. Interline DVR on two same [19] and different voltage distribution lines [20] to restore voltage sag and harmonics has been introduced. When voltage sag and voltage distortion occur on one channel, the DVR on the same channel is able to perform voltage compensation and harmonics elimination, while the other DVR can recharge the energy to the DC-link to maintain the DC-link voltage constant.

In order to efficiently the number of equipment in the DVR circuit configuration, the implementation of a direct ac/ac converter on the DVR has been introduced in [21],[22]. The proposed configuration uses the minimum switches, did not require a dc-link energy storage element, and has a longer compensation time during sag/swell voltage disturbances. The compensation voltage for each phase is taken from each of the three-phase sources so that each converter was able to operate independently and is also able to compensate for single-phase blackouts and unbalance sag/swell voltages. The use of a single-phase Transformerless DVR (TDVR) to mitigate the sag/swell voltage has been observed in [23]. The proposed configuration was capable of reducing system size and losses compared to DVR which using a series transformer. The single-phase interactive channel DVR using the sag voltage detection algorithm has been developed in [24]. The detection algorithm has a hybrid structure consisting of a momentary detection section and a RMS variation detection section. The DVR development could compensate for input voltage sag or interrupt in 2.0-ms delay and can be used effectively for sensitive loads.

The single-phase DVR with synchronous reference frame control under distorted source conditions has been applied in [25]. The proposed control using a moving average filter (MAF) is capable of extracting positive sequence fundamental components as well as being able to mitigate voltages sag and distorted source voltages. The single-phase DVR using elliptical restoration-based voltage compensation to correct the power factor on the source side has been proposed in [26]. The active and reactive voltage components and centrifugal angles are used to formulate an elliptical compensation path. So that the voltage will be in-phase with the load current using precise control of the DVR injection voltage. The optimization of the voltage injection technique in DVR to protect sensitive loads has been observed in [27]. The recursive least square (RLS) method is used to estimate

the magnitude and phase of the voltage in order to minimize the amplitude of the injection voltage. Meanwhile, repetitive control was proposed to track the compensation voltage. Both controls are suitable for sinusoidal reference and are reliable for mitigating harmonics, sags, and swell distortions.

Energy storage in single or three-phase DVR circuits related to the capacity and type of energy storage has become the attention of many researchers. The determination of the two parameters relates to the ability and duration of the energy storage to supply real power to the inverter during a fault. Unbalanced voltage compensation in 3P3W system using DVR using a super capacitor has been investigated in [28]. The proposed DVR configuration uses a control based on the d-q-0 and Proportional Integral (PI) transformation technique and is further coded using a digital signal processor (DSP). DSP control and super capacitor implementation can mitigate unbalanced voltage disturbances. A compressed air energy storage powered dynamic voltage restorer (CAESPDVR) with ANFIS control has been proposed in [29] to compensate for unbalanced sag/swell voltages and harmonics. The single-phase DVR configuration using a hybrid energy storage system (HES) has been developed in [30]. The HES series consists of superconducting magnetic energy storage (SMES) in collaboration with battery energy storage (BES) on a DC type DVR. The proposed HES concept integrated with fast response large power SMES unit and low-cost high capacity BES can further be implemented in large scale DVR development.

In this paper, BES is proposed as energy storage and implemented in single-phase DVR using load voltage control with the UVTG method and connected to linear/non-linear loads. The UVTG method on the DVR system is implemented using the Arduino-Uno microcontroller hardware. The LabVIEW-based interface simulation is used to monitor electrical quantities in real-time during the voltage sag period i.e. source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power factor measurements are also carried out to obtain the total harmonic value or Total Harmonic Distortion (THD) of the source current and load current.

This paper is arranged as follows. Section 2 presents the proposed method, UVTG method, percentage of voltage sag, true power factor and harmonic, single-phase DVR-BES using LabVIEW, as well as hardware and software implementation, Section 3 presents results and discussion of the source voltage, injection voltage, load voltage, DC-link voltage, source current, load current, percentage of voltage sag, true power-factor, and current THD which analyzed from data measured by Arduino-Uno and monitored by LabVIEW. In this section, the system connected to the linear/non-linear load with and without voltage sag is selected to present the best performance single-phase DVR-BES system connected to three different types of load during voltage sag. Finally, this paper is concluded in Section 4.All manuscripts must be in English. These guidelines include complete descriptions of the fonts, spacing, and related information for producing your proceedings manuscripts. Table 1 shows the abbreviations used in this paper.

Table 1. Abbreviation

Symbol	Description
PQ	Power Quality
DVR	Dynamic Voltage Restorer
BES	Battery Energy Storage
UVTG	Unit Vector Template Generation
THD	Total Harmonic Distortion
Pf_{true}	True Power Factor
FL	Fluorescent
LED	Light Emitting Diode
DG	Distributed Generation
3P3W	Three Phase Three Wire
3P4W	Three Phase Four Wire
SPWM	Sinusoidal Pulse Width Modulation
CB	Circuit Breaker
RMS	Root Mean Square
GUI	Graphic User Interface

2. Research Method

2.1. Proposed Method

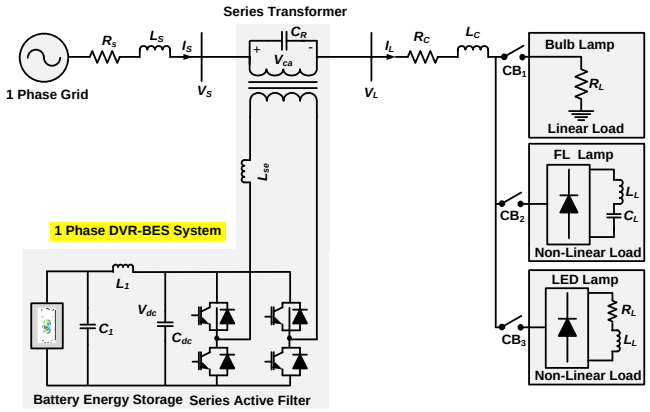

Fig. 1. Proposed single phase DVR-BES connected to linear/non-linear load

Fig. 1 shows a single-phase DVR supplied by BES using load voltage control with the UVTG method. The DVR is a tool that functions to compensate for the load voltage in the event of a voltage sag disturbance on the source bus at a level of 0.1 to 0.9 per unit. The UVTG method on the DVR system is implemented using the Arduino-Uno microcontroller hardware. LabVIEW-based interface simulation is used to monitor electrical quantities in real-time during the voltage sag period i.e. source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power-factor measurements are also carried out to obtain the THD value of the source current and load current. There are two cases in this study, the source without voltage sag, and with an 80% voltage sag. In

each case, the single-phase DVR system is supplied by BES connected to a 5-watt bulb lamp (linear load), 5 watt FL lamp (non-linear load), and 5 watts LED lamp (non-linear load), so the total selected case is six. The CB1, CB2, and CB3 are used to connect and disconnect links to three linear/non-linear loads. The DVR-BES system configuration is then run based on a predetermined case using Arduino-Uno microcontroller interfaced communication and the results are simulated and monitored in real-time by a LabVIEW.

2.1 Unit Voltage Template Generation Method

The series active filter protect sensitive loads against several voltage disturbances from the source bus. In [31], the control method of source and load voltage in a three-phase series active filter has been discussed. Using the same procedure, the authors propose the same method for single-phase series active filter control as shown in Fig. 2. This method extracts UVTG from the distorted input supply. Then, the template is expected to be an ideal sinusoidal signal with a unity amplitude. The source of the distorted voltage is measured and divided by the peak amplitude fundamental input voltage V_m.

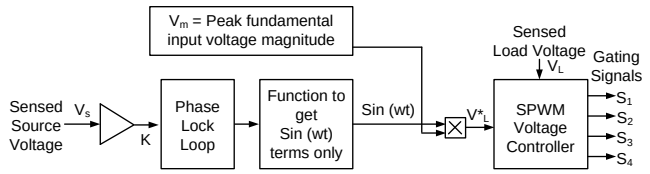

Fig. 2. UVTG control on single phase series active filter

A single-phase locked loop (PLL) is used in order to generate sinusoidal unit vector templates with a phase lagging by the use of the sine equation. The reference signal of the load voltage is calculated by multiplying the unit vector templates with the peak amplitude of the fundamental input voltage V_m. The load reference voltage (V_L^*) is then compared to the sensed load voltage (V_L) by a SPWM controller used to generate the desired four gating signal on a single-phase series active filter.

2.2 Percentage of Voltage Sag

The recommended standard of practice on monitoring voltage sag/swell as part of electric power quality parameters is IEEE 1159 [2]. This standard presents the definition and table of voltage sag base on categories (instantaneous, momentary, temporary) typical duration, and typical magnitude. The percentage of voltage sag is formulated in Eq. (1) [31].

$$Sag\ (\%) = \frac{|Vpre\_sag - V\_sag|}{Vpre\_sag} \quad (1)$$

2.3 True Power Factor and Harmonics

The true power factor at the load is defined as the ratio of average power to apparent power. The true power factor for both sinusoidal and nonsinusoidal situations is presented in Eq. (2) [32].

$$pf_{true} = \frac{P_{avg}}{S} = \frac{P_{avg}}{V_{rms}\, I_{rms}} \quad (2)$$

$$V_{rms} = V_{1rms}\sqrt{1 + (THD_V/100)^2} \quad (3)$$

$$I_{rms} = I_{1rms}\sqrt{1 + (THD_I/100)^2} \quad (4)$$

By substituting Eq. (3) and Eq. (4) into Eq. (2), the true power factor results in Eq. (5) for both sinusoidal and nonsinusoidal cases [32].

$$pf_{true} = \frac{P_{avg}}{V_{1rms}\, I_{1rms}\sqrt{1+(THD_V/100)^2}\sqrt{1+(THD_I/100)^2}} \quad (5)$$

A useful simplification can be made by expressing Eq. (5) as a product of two components defined in Eq. (6).

$$pf_{true} = \frac{P_{avg}}{V_{1rms}\, I_{1rms}} \times \ldots\ldots \frac{1}{\sqrt{1+(THD_V/100)^2}\sqrt{1+(THD_I/100)^2}} \quad (6)$$

By making the following two assumptions: (1) In most cases, the contributions of harmonics above the fundamental to average power are very small, so that is $P_{avg} \approx P_{1avg}$ and (2) Since THD_V is less than 10%, then from (12) we see that $V_{rms} \approx V_{1rms}$. Then, merging both assumptions into Eq. (6) results in the following approximate function for the true power factor presented in Eq. (7) [32].

$$pf_{true} = \frac{P_{1avg}}{V_{1rms}\, I_{1rms}} \times \frac{1}{\sqrt{1+(THD_I/100)^2}} = Pf_{displacement} \times Pf_{distorted} \quad (7)$$

Because displacement power factor (Pf_{disp}) could never be greater than unity, Eq. (7) shows that the true power factor in non-sinusoidal cases has the upper limit so finally its function is defined in Eq. (8).

$$pf_{true} \leq Pf_{distorted} = \frac{1}{\sqrt{1+(THD_I/100)^2}} \quad (8)$$

2.4 Single Phase DVR-BES using LabVIEW

The implementation of the single-phase DVR-BES system consists of several stages. That stage i.e. create a single-phase series active filter, create a gate driver to trigger the MOSFET in the series active filter, create a SPWM program to drive the gate driver as an inverter trigger and create a monitoring program in LabVIEW. Fig. 3 presents a schematic diagram of a single phase DVR-BES system.

Fig. 3 shows that the BES and series active filters play an important role in compensating for the voltage sag on a single-phase DVR. The step-up transformer that is installed in a series against the load functions to inject the voltage from the series active filter to the load. The main energy source for series active filters uses BES DC voltage 12 V with a capacity of 7.2 Ah. The process of changing the DC to AC voltage begins with the Arduino Nano SPWM microcontroller providing Sinusoidal SPWM pulses to the Gate Driver circuit which has the main component of the TLP 250 Optocoupler IC, then the Gate Driver circuit triggers the IRFP250 MOSFET gate on a series active filter circuit cross-like as an electric current cycle in the circuit bridge diode rectifier. So that it will produce an AC output from a series active filter circuit. The output voltage of the series active filter is an AC voltage of 7 V depending on the battery voltage conditions, which will then be increased to an AC voltage of 220 V using a step-up transformer. The step-up series transformer has a power of 600 VA with a primary AC input voltage of 7.2 V and a secondary AC output voltage of 220 V. The goal is that the series active filter is able to inject enough power to compensate for the sag voltage at a level of 10% to 90%.

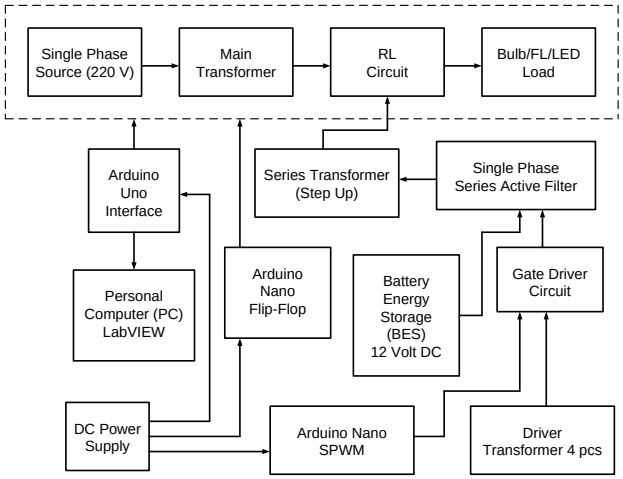

Fig. 3. A schematic diagram of single phase DVR-BES

The Arduino Nano flip-flop functions as a timer to run system simulations using a single-phase DVR-BES without and with sag voltage. The Arduino nano has been programmed with a flip-flop program with the 1-second case instructing the relay to turn "on" as a representation of the system experiencing sag voltage and 1 second ordering the relay to turn "off" as a representation of the system without experiencing sag voltage. This timer is expected to function when there is a sag voltage and automatically orders a single-phase active filter to inject a voltage compensation into the load so that the load voltage will remain stable.

The Arduino Uno interface functions as a medium for receiving data from voltage sensors and current sensors that are measuring the amount of electricity in the DVR circuit and sending the data to a personal computer (PC) with LabVIEW software. Curves and data displayed in LabVIEW i.e. source voltage, load voltage, injection voltage, DC-link voltage, source current, and load current respectively. The display form implemented in LabVIEW is in the form of graphs and number indicators. With a graphic display, the reader will find it easier to observe the wave condition both voltage and current during the system condition without and with voltage sag. All data displayed in LabVIEW is real-time and continuous data as long as the single-phase DVR-BES system is operated to the system. In addition to using the LabVIEW, data collection is also carried out by the cos-phi meter to determine the value of the true power factor of source and load as a basis for determining the harmonic of source and load currents. The single-phase DVR-BES system connected to three linear/non-linear loads i.e. bulb lamp 5 W (linear), FL lamp 5 W (non-linear), LED lamp 5 W (non-linear) respectively.

2.5 Hardware and Software Implementation

The LabVIEW interface software diagram consists of the main program in the form of a Graphic User Interface (GUI) which functions to run all indicators and controls on the front panel. Fig. 4 shows the model of the single-phase DVR-BES hardware circuit. The nominal parameter is presented in Table 2.

Table 2. Nominal of device parameter

Devices	Design Values
Single phase source voltage	220 V
Frequency	50 Hz
Series transformer (*step-up)*	600 VA 7,2/220 V
Main transformer (CT)	3 A
Current sensor ACS 712	5A
Relay	1 device
Arduino uno (Interface)	1 device
Arduino nano (Flip-Flop)	1 device
Arduino nano (SPWM))	1 device
Load resistor	0.4 ohm
Load inductor	15 mH
Cos-phi-meter	1 device
Battery	12 V/7.2 Ah
DC-link capacitor	1000 μF
Bulb lamp load	5 W
FL lamp load	5 W
LED lamp load	5 W

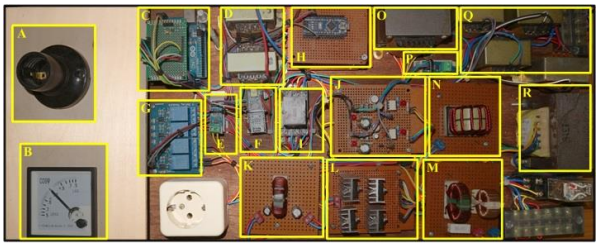

Fig. 4. Single-phase DVR-BES hardware

Where A: Load; B: Cos-phi-meter; C: Arduino Uno; D: Voltage sensor transformer; E: Current sensor; F: Arduino nano SPWM; G: Relay 1 (4 Channel); H: Arduino nano flip-flop; I: Two relays (220V-AC); J: Gate driver optocoupler; K: Series active filter (C_{DC}, L_1, C_1) ; L: Series active filter; M: Load impedance (R_C, L_C); (R_C, L_C); N: Series transformer filter (L_{SC}); O: Main transformer; P: Source current sensor; Q: Gate driver transformer; R: Series transformer.

Fig. 5 shows the overall GUI program design and the component parts of the single-phase DVR-BES. In order for the LabVIEW software interface on the PC to communicate with the Arduino Uno, a program is needed to communicate the two devices. The communication program used by Lifa Base. Lifa Base is the driver for Arduino Uno in connecting data communication with PC. Lifa Base is the default program from Arduino when users install LabVIEW.

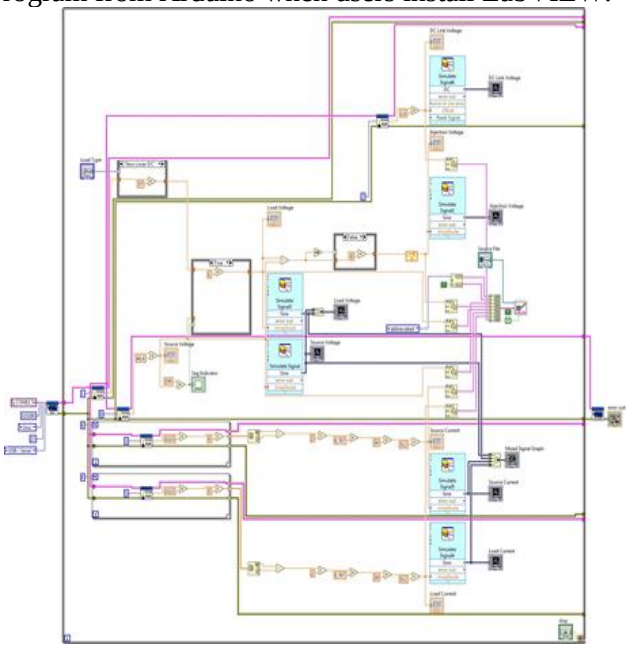

Fig. 5. Software design using LabVIEW interface

3. Results and Discussion

Fig. 1 shows a series of DVR supplied by BES connected to a load of Bulb, FL, and LED respectively. The series transformer connected to the load functions to inject the voltage from the series active filter during voltage sag disturbance. The Arduino Nano Flip-Flop is used as a timer to run simulated data collection. The cycle timer applied to the DVR is 1 second on and 1 second off. The data collection period is carried out with a LabVIEW simulation for 3 seconds, with a sag voltage duration of 80% between 1 second to 2 seconds. Data collection is carried out at 1.5 seconds from the curve of the source voltage (V_S), injection voltage (V_{inj}), load voltage (V_L), DC-link voltage $(V_{DC-Link})$, source current (I_S), and load current (I_L), curves. The true power-factor (Pf_{true}) data in the source bus and load bus is measured from the cos-phi meter.

Using the same LabVIEW simulation procedure and period, data collection is also carried out without the voltage sag. Percentage of load voltage sag is calculated using Eq. (1) with a pre-sag voltage of 203 V. Base on true power-factor, then harmonics current is measured using Eq. (8). Table 3 presents the performance of voltage, current, and sag percentage of the single-phase DVR supplied by BES without and with voltage sag disturbance. Table 4 presents the performance of true power factor and harmonics of the single-phase DVR supplied by BES without and with voltage sag disturbance. Fig. 6, Fig. 7, and Fig. 8 show curves of voltage, current, and sag percentage of the single-phase DVR supplied by BES connecting to bulb lamp, FL lamp, and LED lamp load respectively.

Table 3. Performance of voltage, current, and sag percentage of the single-phase DVR supplied by BES

No.	Load Type	V_S (V)	$V_{Inj}(V)$	V_L (V)	I_S (A)	I_L (A)	$V_{DC-Link}$ (V)	Sag (%)
Without Voltage Sag								
1.	Bulb Lamp	203	0	203	0.208	0.166	13.03	0
2.	FL Lamp	203	0	203	0.208	0.083	13.03	0
3.	LED Lamp	203	0	203	0.270	0.166	13.03	0
With Sag Voltage								
4.	Bulb Lamp	44.7	168	216	0.228	0.145	8.20	6.40
5.	FL Lamp	50.3	200	256	0.166	0.208	7.33	26.13
6.	LED Lamp	49.1	133	185	0.249	0.789	8.06	8.87

Table 4. Performance of power factor and harmonics of the single-phase DVR supplied by BES

No.	Load Type	Pf_S	Pf_L	THD_S (%)	THD_L (%)
Without Voltage Sag					
1.	Bulb Lamp	0.850	0.999	17.647	0.1001
2.	FL Lamp	0.900	0.999	11.111	0.1001
3.	LED Lamp	0.990	0.999	1.010	0.1001
With Sag Voltage					
4.	Bulb Lamp	0.985	0.998	1.523	0.2040
5.	FL Lamp	0.985	0.994	1.523	0.6040
6.	LED Lamp	0.990	0.975	1.010	2.5640

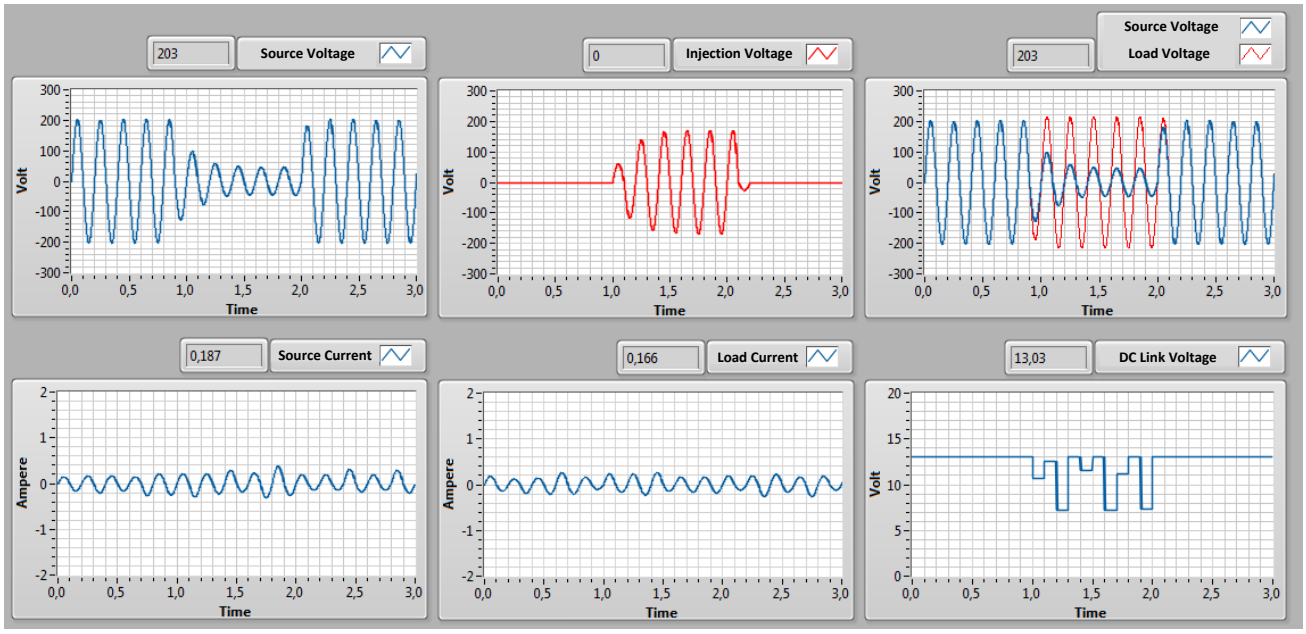

Fig. 6. Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to bulb lamp load using LabVIEW

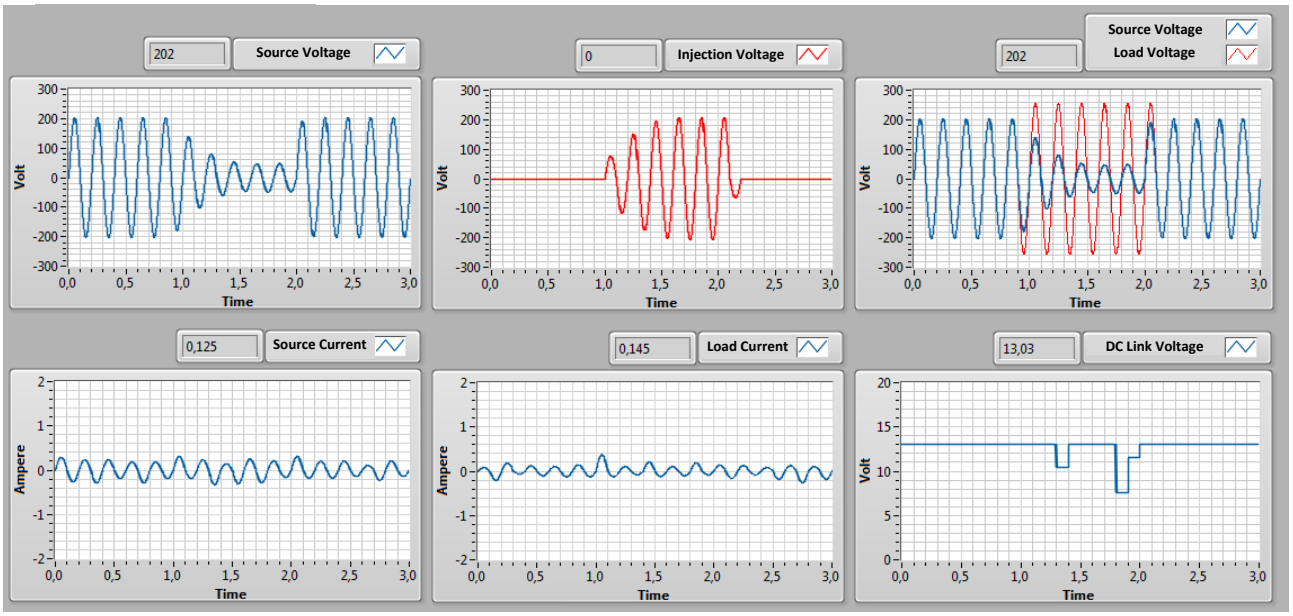

Fig. 7. Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to FL lamp load using LabVIEW

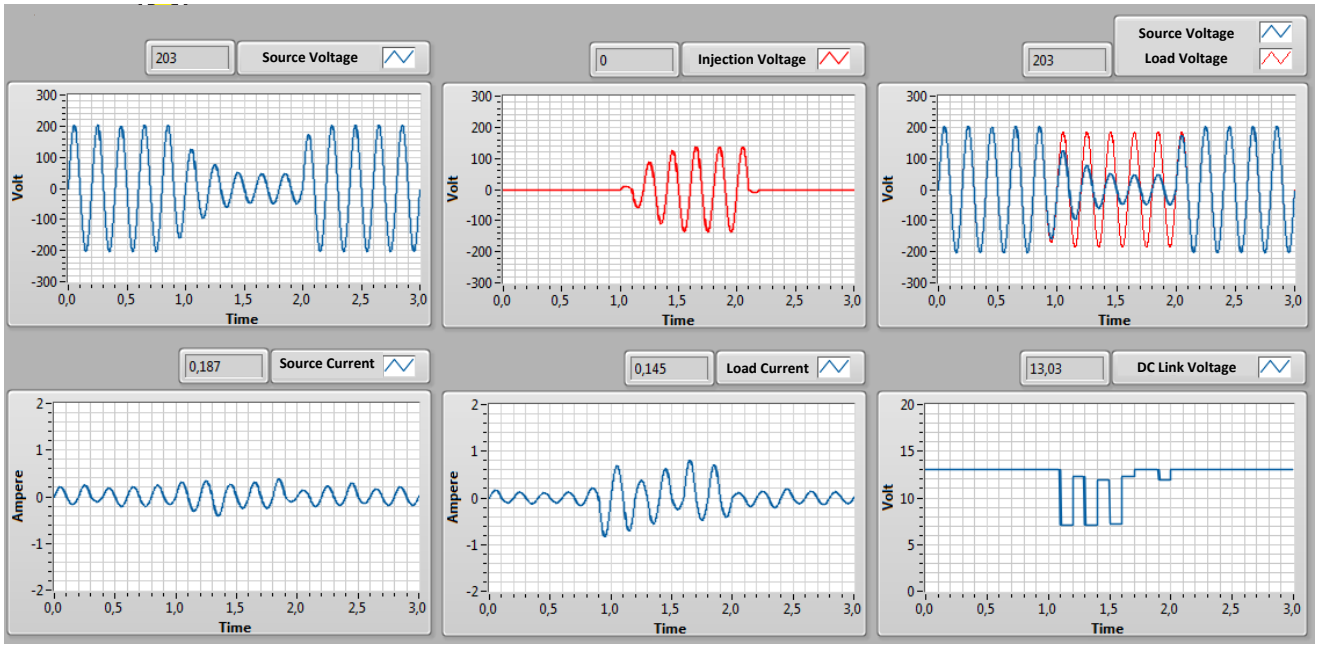

Fig. 8. Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to LED lamp load using LabVIEW

Fig. 6 shows the simulation curve of the sag voltage on a single-phase DVR system supplied by a BES connected to a bulb lamp load. The voltage sag disturbance lasts from t = 1 to t = 2 seconds with a total simulation time of 3 seconds. The measurements on all simulation parameters curves are carried out at seconds t = 0.5 seconds. At t = 1, the source voltage (V_S) drops from 230 V to 44.7 V, and the series transformer injects a voltage (V_{Inj}) of 168 V so that the load voltage (V_L) remains constant at 216 V. In this disturbance condition the value of the source current (I_S) is 0.228 A and the load current (I_L) drops to 0.45 A. To keep the load voltage (V_L) maintain constant, BES releases its energy so that the DC link voltage($V_{DC-Link}$) drops from 13.03 V to 8.20 V.

Fig. 7 shows the simulation curve of sag voltage on a single-phase DVR system supplied by the connected BES to the FL lamp load. At t = 1 the source voltage (V_S) drops from 230 V to 50.3 V and the series transformer injects a voltage (V_{Inj}) of 200 V, so that the load voltage (V_L) remains constant at 256 V. During the duration of the sag voltage, the capacitance effect of the capacitor component able to store charge on the FL lamp load, causing the load voltage value to exceed the source voltage. In the disturbance conditions, the value of the source current (I_S) is 0.166 A and the load current drops to 0.208 A. To keep the load voltage maintain constant, BES releases its energy so that the DC link voltage ($V_{DC-Link}$) drops from 13.03 V to 7.33 V.

Fig. 8 shows a simulation curve voltage sag on a single-phase DVR system supplied by BES connects to the LED lamp load. At t = 1 the source voltage (V_S) drops from 230 V to 49.1 V and the series transformer injects a voltage (V_{Inj}) of 133 V so that the load voltage (V_L) remains constant at 185 V. During the disturbance conditions, the value of the source current (I_S) is 0.249 A, and the load current increases to 0.789 A. To keep the load voltage maintain constant, BES then releases its energy so that the DC link voltage ($V_{DC-Link}$) drops from 13.03 V to 8.06 V.

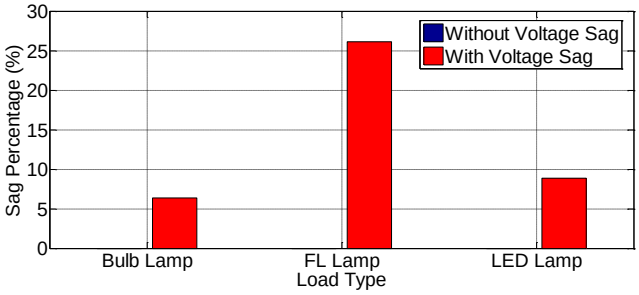

Fig. 9. Performance of sag percentage for single phase DVR-BES system on three load type

Fig. 9 shows that for the system without sag voltage, the series active filter circuit and series transformer on a single-phase DVR-BES system is not able to inject voltage into the load, so produces a percentage change in load voltage of 0%. Otherwise if the system with sag voltage, the single-phase DVR-BES system is able to maintain the load voltage i.e. bulb lamp, FL lamp, and LED lamp of 216 V, 256 V, and 185 V, respectively. The percentage of load voltage disturbance for the system with sag voltage

for the three loads type are 6.4%, 26.13%, and 8.87%, respectively.

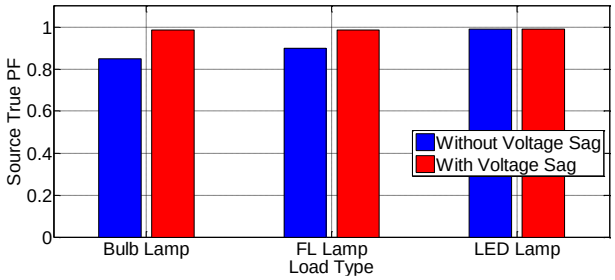

Fig. 10. Performance of source true power-factor for single phase DVR-BES system on three load type

Fig. 10 shows the measurement of source true power-factor without voltage sag of the bulb lamp has the worst true power-factor (Pf_{true}) of 0.850 leading compared to a FL lamp of 0.900 leading and an LED lamp of 0.909 leading. Otherwise for the system with voltage sag, the single-phase DVR-BES system produces source true power factor (Pf_{true}) for a bulb lamp, FL lamp, and LED lamp of 0.985 leading, 0.985 leading, and 0.990 leading respectively.

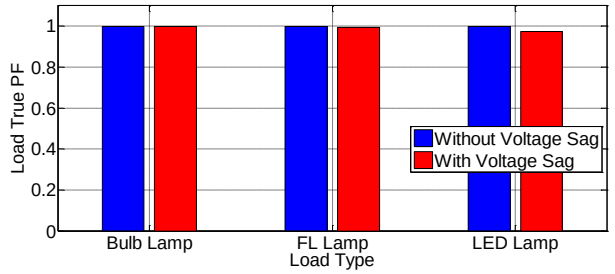

Fig. 11. Performance of load true power-factor for single phase DVR-BES system on three load type

Fig. 11 shows the measurement of load power-factor without voltage sag for all load categories results in the same true power factor (Pf_{true}) of 0.999 leading. Otherwise, for the system with voltage sag is able to result load true power factor (Pf_{true}) i.e. bulb lamp, FL lamp, and LED lamp of 0.975 leading, 0.998 leading, and 0.994 leading respectively.

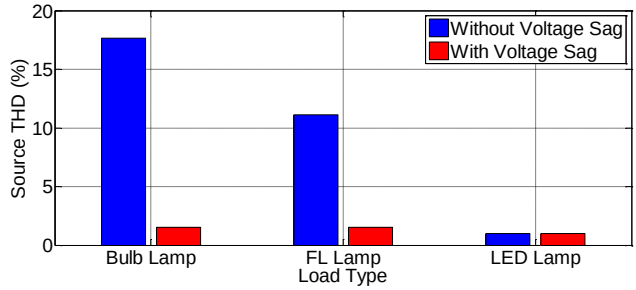

Fig. 12. Performance of source harmonics for single phase DVR-BES system on three load type

Fig. 12 shows that the system without sag voltage is able to produce the source THD for bulb lamp, FL lamp, and LED lamp of 17.647%, 11.111%, and 1.010% respectively. Otherwise, for the same system with sag voltage is able to result source THD for bulb lamp, FL lamp, and LED lamp of 1.523%, 1.523%, and 1.010% respectively.

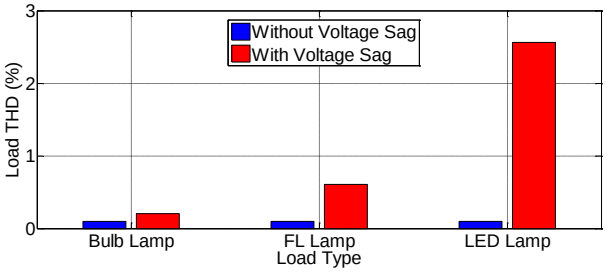

Fig. 13. Performance of load harmonics for single phase DVR-BES system on three load type

Fig. 13 shows that the system without voltage sag is able to produce the same load THD for bulb lamp, FL lamp, and LED lamp of 0.1001%. Otherwise, for the same system with voltage sag is able to result load THD for bulb lamp, FL lamp, and LED lamp of 0.204%, 0.604%, and 2.564% respectively. Fig 10 and Fig. 11 shows in the case of voltage sag and three types of loads, the LHE lamp is able to result in the best performance because it is able to produce the highest source true power factor of 0.990 and the lowest source current THD of 1.010%. The THD value of source current and load current in voltage sag also had met the IEEE 519.

4. Conclusion

The system using a single-phase DVR supplied by BES with load voltage controlled by a UVTG method has been implemented. The model is connected to three types of linear/non-linear load i.e. bulb lamp, FL lamp, and LED lamp. This configuration is proposed to mitigate 80% voltage sag using the Arduino-Uno hardware and monitored by LabVIEW simulation in real-time. The investigated parameter are source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power-factor measurements are also carried out to obtain the harmonics of the source current and load current. During voltage sag, the single-phase DVR-BES system is able to maintain load voltage for all types of loads. From the system with voltage sag and three different types of loads, the LHE lamp is able to result in the best performance because it is able to produce the highest source current power factor and the lowest source current THD. The THD value of source and load current with voltage sag also had met the IEEE 519.

In a system using a single-phase DVR-BES connected to the FL load, there is a significant increase in load voltage of 256 V compared to the source voltage. The percentage of sag voltage for FL lamps also increased by 26.13% and has far exceeded

the value of 5%. The implementation of a single-phase bidirectional inverter circuit as the interface between the BES and series active filters can be proposed as future work to overcome this problem.

Conflicts of Interest

The authors declare no conflict of interest.

Author Contributions

Conceptualization, Y.A. Setiawan and A. Amirullah; methodology, Y.A. Setiawan and A. Amirullah; software, Y.A. Setiawan; validation, Y.A. Setiawan; formal analysis, Y.A. Setiawan and A. Amirullah; investigation, Y.A. Setiawan and A. Amirullah; resources, Y.A. Setiawan; data curation, Y.A. Setiawan; writing—original draft preparation, Y.A. Setiawan; writing—review and editing, Y.A. Setiawan; visualization, Y.A. Setiawan; supervision, A. Amirullah; project administration, Y.A. Setiawan; funding acquisition, A.Amirullah. All authors read and approved the final manuscript.

Acknowledgements

The authors would like to acknowledge to Institutions of Research and Community Service Universitas Bhayangkara Surabaya, for funding to this research base on Decree Letter Number 65/XI/2020/UBHARA date 19 November 2020.

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Lampiran 2.2

Cover Letter

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Paper Title	**Implementation of Single-Phase DVR-BES Based on Unit Vector Template Generation (UVTG) to Mitigate Voltage Sag Using Arduino Uno and Monitored in Real-Time Through LabVIEW Simulation**
Co-author(s)	**Yohanes Artha Setiawan**
Organization	**Electrical Engineering Study Program, Faculty of Engineering, Universitas Bhayangkara Surabaya, Surabaya 60231**
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International Journal of Intelligent Engineering and Systems (IJIES)

Paper ID	Ijies3819
Paper Title	Implementation of Single-Phase DVR-BES Based on Unit Vector Template Generation (UVTG) to Mitigate Voltage Sag Using Arduino Uno and Monitored in Real-Time Through LabVIEW Simulation

Recommendation for Publication

~~□(Evaluation A:) Accept~~ ~~□(Evaluation B:) Accept after Minor Revision~~

□(Evaluation C:) Accept after Major Revision ~~□(Evaluation D:) Reject~~

Comments from reviewers 1 & 2:

1. By quoting the authors' previous works, such as
   Amirullah Amirullah et al. "Load active power transfer enhancement using UPQC-PV-BES system with fuzzy logic controller", International Journal of Intelligent Engineering and Systems, Vol.13, No.2, 2020 DOI: 10.22266/ijies2020.0430.32,
   the authors should clarify the position of this research.
2. What's "All manuscripts must be in English. These guidelines include complete descriptions of the fonts, spacing, and related information for producing your proceedings manuscripts" in p. 2?
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[1] R. Ruskone, S. Airault, and O. Jamet, "Vehicle Detection on Aerial Images", *International Journal of*

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[2] R. Ruskone, L. Guigues, S. Airault, and O. Jamet, "Vehicle Detection on Aerial Images", In: *Proc. of International Conf. On Pattern Recognition*, Vienna, Austria, pp.900-904, 1996.

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Response Letter

Ijies3819 Reply Form:

Paper ID	**Ijies3819**
Paper Title	**Implementation of Single-Phase DVR-BES Based on Unit Vector Template Generation (UVTG) to Mitigate Voltage Sag Using Arduino Uno and Monitored in Real-Time Through LabVIEW Simulation**

Reviewer comment to the authors:

1. By quoting the authors' previous works, such as
   Amirullah Amirullah et al. "Load active power transfer enhancement using UPQC-PV-BES system with fuzzy logic controller", International Journal of Intelligent Engineering and Systems, Vol.13, No.2, 2020 DOI: 10.22266/ijies2020.0430.32,
   the authors should clarify the position of this research.

Answer:

Thanks a lot you for your valuable comment.

1. The answers to question number 1 are below:
   a. The paper entitled Amirullah Amirullah, Adiananda Adiananda, Ontoseno Penangsang, and Adi Soeprijanto, "Load active power transfer enhancement using UPQC-PV-BES system with fuzzy logic controller", International Journal of Intelligent Engineering and Systems, Vol.13, No.2, 2020 DOI: 10.22266/ijies2020.0430.32, link: **http://www.inass.org/2020/2020043032.pdf** was the outcome from Fundamental Research accordance with the Decree Letter Number: 7/E/KPT/2019 and Contract Number: 229/SP2H/DRPM/2019 on 11 March 2019, 008/SP2H/LT/MULTI/L7/2019 on 26 March 2019, and 170/LPPM/IV/2019/UB on 4 April 2019. This research was financially supported by The Directorate General of Research and Development Strengthening, Directorate of Research and Community Service, Ministry of Research, Technology, and Higher Education, the Republic of Indonesia **(See Acknowledgments Section of the paper on Page 19).** My position in this research was the main (1st) author (researcher) and also the corresponding author. Adiananda Adiananda, Ontoseno Penangsang, and Adi Soeprijanto are the 2nd, 3rd, and 4th authors. Adiananda Adiananda is my lecturer colleague in the Electrical Engineering Study Program, Faculty of Engineering Universitas Bhayangkara Surabaya Indonesia. Professor Ontoseno Penangsang and Professor Adi Soeprijanto were my supervisors when I was pursuing a Ph.D in the Department of Electrical Engineering, Faculty of Intelligent Electrical and Informatics Technology, Institut Teknologi Sepuluh Nopember, Surabaya, Indonesia for the period of 2014-2019. I have chosen and written Professor Ontoseno and Profesor Adi as the 3rd and 4th authors in this paper, because this research was still related and was a continuation of the major topic of my Ph.D dissertation entitled "The Mitigation of Power Quality Problems Using Unified Power Quality (UPQC) and Battery Energy Storage Supplied by Hybrid Renewable Energy Generator based Artificial Intelligent". The

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iv. Adi Soeprijanto,

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The biographies of the authors in this paper are:

	**Amirullah** was born in Sampang East Java Indonesia, in 1977. He received B.Eng and M.Eng degrees in electrical engineering from the University of Brawijaya Malang and ITS Surabaya, in 2000 and 2008, respectively. Since 2002, He also has worked as a lecturer in Universitas Bhayangkara Surabaya. He obtained a Doctoral degree from electrical engineering ITS Surabaya in 2019 from Power System and Simulation Laboratory (PSSL). He has 12 publications in Scopus with h-index 4. His research interest includes power distribution modelling and simulation, power quality, harmonics mitigation, design of filter/power factor correction, and renewable energy base on artificial intelligence. He also has been an IEEE member since 2019.
	**Adiananda** was born in Nganjuk East Java Indonesia, in 1973. He received bachelor degree in electrical engineering from Universitas Bhayangkara Surabaya and a master of computer science from Gadjah Mada University (UGM) Yogyakarta, in 1996 and 2016, respectively. Since 1998, He has worked as a lecturer in Universitas Bhayangkara Surabaya. He is interested in the research of the application of artificial intelligence in modelling power electronics and computer systems.
	**Ontoseno Penangsang** was born in Madiun East Java Indonesia, in 1949. He received a bachelor in electrical engineering from ITS Surabaya, in 1974. He received and M.Sc. and Ph.D. degree in Power System Analysis from the University of Wisconsin, Madison, USA, in 1979 and 1983, respectively. He is currently a professor at the Department of Electrical Engineering and ITS Surabaya. He has a long experience and main interest in power system analysis (with renewable energy sources), design of power distribution, power quality, and harmonic mitigation in industry. Professor Ontoseno Penangsang has 76 publications in Scopus with h-index 8.
	**Adi Soeprijanto** was born in Lumajang East Java Indonesia, in 1964. He received a bachelor in electrical engineering from ITB Bandung, in 1988. He received a master of electrical engineering in control automatic from ITB Bandung. He continued his study to Doctoral Program in Power System Control at Hiroshima University Japan and was finished it's in 2001. He is currently a professor at the Department of Electrical Engineering and a member of PSSL in ITS Surabaya. His main interest includes power system analysis, power system stability control, and power system dynamic stability. He had already achieved a patent in the optimum operation of the power system. Professor Adi Soeprijanto has 141 publications in Scopus with h-index 12.

b. The paper entitled "Yohanes Artha Setiawan and Amirullah Amirullah, Implementation of

Single-Phase DVR-BES Based on Unit Vector Template Generation (UVTG) to Mitigate Voltage Sag Using Arduino Uno and Monitored in Real-Time Through LabVIEW Simulation" (Paper ID: Ijies3819) was the outcome of bachelor theses from Yohanes Artha Setiawan last year. I was a thesis supervisor for 8 months from January to August 2020. Now, Yohanes has graduated and has worked for a private company in Surabaya, Indonesia. In accordance with our university regulations, because the research was Yohanes's work, he had the right to be the first author, and I was as his supervisor selected to be the second author (also as a corresponding author). My consideration chooses as the corresponding author was because Yohanes's ability to write papers in English relatively limited, so I helped him to write and to submit the results for publication in English to the International Journal of Intelligent Engineering and Systems (IJIES) including communication with the editor for its progress (also revision of this paper). **The Author Contributions are** Conceptualization, Y.A. Setiawan and A. Amirullah; methodology, Y.A. Setiawan and A. Amirullah; software, Y.A. Setiawan; validation, Y.A. Setiawan; formal analysis, Y.A. Setiawan and A. Amirullah; investigation, Y.A. Setiawan and A. Amirullah; resources, Y.A. Setiawan; data curation, Y.A. Setiawan; writing—original draft preparation, Y.A. Setiawan; writing—review and editing, Y.A. Setiawan; visualization, Y.A. Setiawan; supervision, A. Amirullah; project administration, Y.A. Setiawan; funding acquisition, A.Amirullah. All authors read and approved the final manuscript **(See Author Contributions Section of Paper ID: Ijies3819 on Page 12).**

The biographies of the authors in this paper (IJIES Paper ID: Ijies3819)" are:

	**Yohanes Artha Setiawan** was born in Surabaya, in 1996. He just has received B.Eng degree in electrical engineering from Universitas Bhayangkara Surabaya in 2019. His research interest i.e. design and implementation of power electronics circuit control method, power quality, harmonics mitigation, active-passive filter, and power factor correction system on the low voltage distribution system.
	**Amirullah** was born in Sampang East Java Indonesia, in 1977. He received B.Eng and M.Eng degrees in electrical engineering from the University of Brawijaya Malang and ITS Surabaya, in 2000 and 2008, respectively. Since 2002, He also has worked as a lecturer in Universitas Bhayangkara Surabaya. He obtained a Doctoral degree from electrical engineering ITS Surabaya in 2019 from Power System and Simulation Laboratory (PSSL). He has 12 publications in Scopus with h-index 4. His research interest includes power distribution modelling and simulation, power quality, harmonics mitigation, design of filter/power factor correction, and renewable energy base on artificial intelligence. He also has been an IEEE member since 2019.

Reviewer comment to the authors:

2. What's "All manuscripts must be in English. These guidelines include complete descriptions of the fonts, spacing, and related information for producing your proceedings manuscripts" in p. 2?

Answer:

Thanks a lot for your valuable comment.

1. The answers to question number 2 are below:
   a. The authors have revised "Fig" to "Figure" started Figure 1 to Figure 13 below:(See Page 5 to Page 10 and Red Font)
      i. Figure. 1 Proposed single phase DVR-BES connected to linear/non-linear load.
      ii. Figure. 2 UVTG control on single phase series active filter
      iii. Figure. 3 A schematic diagram of single phase DVR-BES
      iv. Figure. 4 Single-phase DVR-BES hardware
      v. Figure. 5 Software design using LabVIEW interface for simulate signal i.e. (A) arduino-uno data communication, (B) source voltage (V_S), (C) injected voltage (V_{Inj}), (D) load voltage (V_{Inj}), (E) source current (I_S), (F) load current (I_L), (G) DC-link voltage ($V_{DC-Link}$), and (H) mixed signal graph
      vi. Figure. 6 Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to bulb lamp load using LabVIEW
      vii. Figure. 7 Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to FL lamp load using LabVIEW
      viii. Figure. 8 Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to LED lamp load using LabVIEW
      ix. Figure. 9 Performance of sag deviation of V_L for single phase DVR-BES system on three load type
      x. Figure.10 Performance of source true power-factor for single phase DVR-BES system on three load type
      xi. Figure. 11 Performance of load true power-factor for single phase DVR-BES system on three load type
      xii. Figure. 12 Performance of source harmonics for single phase DVR-BES system on three load type
      xiii. Figure. 13 Performance of load harmonics for single phase DVR-BES system on three load type
   b. The authors have revised the font "2. Research Method" and "2.1. Proposed Method" from "Garamond" to "Times New Roman" base on IJIES Format Manuscript on Page 2 (See Page 4 and Red Font

Reviewer comment to the authors:

3. There is no explanation about the parameters shown in Fig. 1. The authors should clarify it.

Answer:

Thanks a lot for your valuable comment.

3. The authors have added Table 2 to shows the notation list and parameters of Fig. 1 (See Page 4, Column 1, and Column 2, Red Font in the manuscript).

Table 2. Notation list and parameters

(See notation, description, and parameter of Fig 1 in Red Font below)

Notation	Description
V_S	Source Voltage
V_{inj}	Injection Voltage
V_L	Load Voltage
$V_{DC-Link}$	DC-Link Voltage
I_S	Source Current
I_L	Load Current
I_L^*	Reference Load Voltage
V_m	Peak Fundamental Input Voltage Magnitude
K	Gain
S_1, S_2, S_3, S_4	Gating Signal 1, 2, 3, and 4
Sag_{dev}	Voltage Sag Deviation
$V_{pre-sag}$	Pre-Sag Voltage
V_{sag}	Sag Voltage
Pf_{true}	True Power Factor
P_{avg}	Average Power
S	Apparent Power
V_{rms}	RMS Voltage
I_{rms}	RMS Current
V_{1rms}	RMS Fundamental Voltage
I_{1rms}	RMS Fundamental Current
THD_V	Voltage THD
THD_I	Current THD
P_{1avg}	Fundamental Average Power
$Pf_{displacement}$	Displacement Power Factor
$Pf_{distorted}$	Distorted Power Factor
R_S	Line Resistance (0.1 ohm)
L_S	Line Inductance (0.15 mH)
R_C	Load Resistance (0.4 ohm)
L_C	Load Inductance (15 mH)
L_{Se}	Series Inductance (0.015 mH)
L_1	BES Inductance (6 mH)
C_1	BES Capacitance (1000 µF)
C_{DC}	DC-Link Capacitance (200 µF)
R_L	Linier/Non-Linear Resistance (0.6 ohm)
L_L	Non-Linear Load Inductance (0.15 mH)
C_L	Non-Linear Load Capacitance (3.3 µF)
C_R	Ripple Capacitance (0.2 µF)

Reviewer comment to the authors:

4. The explanation about the mathematical formulas is not enough. Furthermore, the meaning of variables and suffix is not clear. Readers will be confused. To help readers' understanding, the authors should add a notation list.

Answer:

Thanks a lot for your valuable comment.

4. The authors have added notation lists and parameters in Table 2 to explain the mathematical formulas as well as the meaning of variables and suffix. (See Page 4, Column 1, and Column 2, Red Font in the manuscript).

Table 2. Notation list and parameters

(See notation and description of a mathematical formula in Red Font below)

Notation	Description
V_S	Source Voltage
V_{inj}	Injection Voltage
V_L	Load Voltage
$V_{DC-Link}$	DC-Link Voltage
I_S	Source Current
I_L	Load Current
I_L^*	Reference Load Voltage
V_m	Peak Fundamental Input Voltage Magnitude
K	Gain
S_1, S_2, S_3, S_4	Gating Signal 1, 2, 3, and 4
Sag_{dev}	Voltage Sag Deviation
$V_{pre-sag}$	Pre-Sag Voltage
V_{sag}	Sag Voltage
Pf_{true}	True Power Factor
P_{avg}	Average Power
S	Apparent Power
V_{rms}	RMS Voltage
I_{rms}	RMS Current
V_{1rms}	RMS Fundamental Voltage
I_{1rms}	RMS Fundamental Current
THD_V	Voltage THD
THD_I	Current THD
P_{1avg}	Fundamental Average Power
$Pf_{displacement}$	Displacement Power Factor
$Pf_{distorted}$	Distorted Power Factor
R_S	Line Resistance (0.1 ohm)
L_S	Line Inductance (0.15 mH)
R_C	Load Resistance (0.4 ohm)
L_C	Load Inductance (15 mH)
L_{Se}	Series Inductance (0.015 mH)
L_1	BES Inductance (6 mH)
C_1	BES Capacitance (1000 µF)
C_{DC}	DC-Link Capacitance (200 µF)
R_L	Linier/Non-Linear Resistance (0.6 ohm)
L_L	Non-Linear Load Inductance (0.15 mH)
C_L	Non-Linear Load Capacitance (3.3 µF)
C_R	Ripple Capacitance (0.2 µF)

Reviewer comment to the authors:

5. Overall, the authors have made a good attempt. However, the authors' proposed method does not adequately describe their data. The results are not supported by any theoretical/mathematical reasons. Readers will fail to understand the scientific contribution of this research. The authors should justify the effectiveness of the proposed technique theoretically.

Answer:

Thanks a lot you for your valuable comment.

5. The answers to question number 5 are below:
   a. The authors have added Table 6. Comparison of implementation UVTG-DVR-BES-Arduino-Uno-LabVIEW (proposed study) and previous studies, to show the effectiveness of the proposed technique theoretically and contribution of research. The parameters observed are depth sag of V_S, sag deviation of V_L, load THD_V, source THD_I, and real-time simulation. (See Page 6 and Red Font).
   b. The authors also have explained the effectiveness of the proposed technique theoretically and contribution of research in two paragraph below Table 6.
   c. The main contribution of this research: "The proposed study is able to give the best performance because it is able to produce source THD_I lower than [28] and source pf_{true} is higher than [26]. Another contribution is that by using the Arduino-Uno interface, the proposed model can be run and monitored in real-time with LabVIEW. It is different from the simulations conducted by 12 previous researchers (except [31]) which were still carried out off-line using Matlab/Simulink environment" (See this explanation in Page 12, The End of Paragraph 1 column 1 and 2, Red Font)

Table 6 and Its Explanatory Paragraphs

Table 6. Comparison of implementation UVTG-DVR-BES-Arduino-Uno-LabVIEW (proposed study) and previous studies

No.	Authors	Methods	Depth Sag of V_S (%)	Sag Dev of V_L(%)	Load THD_V (%)	Source THD_I(%)	Source pf_{true}	Real Time
1	D.N. Katole, et.al [8]	Improved SRF	42	7.6	NA	NA	NA	Not
2	M.T. Hagh, et.al. [10]	FLC	92 without and 95 with DG	8.9 without DG and 6.4 with DG	1.26 without DG and 3.54 with DG	NA	NA	Not
3	H.K. Yada, et. al [16]	SOGI-PLL	30	3.0	NA	NA	NA	Not
4	S. Galeshi, et. al. [17]	Multilevel Cascade H-Bridge Inverter	20	0.0	4.0	NA	NA	Not
5	R. Nittala, et.al [19]	IDVR with VSI and CSI	27.7 with VSI and CSI	0 with VSI and CSI	0.06 with VSI and 0.05 with CSI	NA	NA	Not
6	E. Babaei, et. al. [22]	Direct Converter	65	0	7.07 (Average)	NA	NA	Not

7	A. Benhail, et.al. [23]	TDVR-PI	30	2.18	24	NA	NA	Not
8	J. Ye, et.al. [26]	Elliptical Restoration	60	NA	NA	NA	0.75	Not
9	R. Omar, et.al [28]	DVR-Super-capacitor	30	0	NA	2.38	NA	Not
10	C.K. Sundara-balan, et. al. [29]	CAESPDVR-ANFIS	46.67 (Average)	0.4	2.35	NA	NA	Not
11	V.K. Awaar, et.al. [31]	VSI-SPWM-NI-myRIO-1900-Labview	50	8.79	NA	NA	NA	Yes
12	A.Kiswantono et.al. [32]	UVTG-DVR-BES-PV	80	2.89 (Average)	5.81 (Average)	NA	NA	Not
13	**Proposed Study**	**UVTG-DVR-BES-Arduino-Uno-Labview**	**80**	**Bulb=6.4 FL =26.13 LED=8.87**	**NA**	**Bulb=1.523 FL=1.523 LED=1.010**	**Bulb=0.985 FL=0.985 LED=0.990**	**Yes**

Note: NA = note available

Table 6 shows the validation of the results for the proposed study compared to the 12 previous studies. The parameters observed are depth of sag of V_S, sag deviation of V_L, load THD_V, source THD_I, and real-time simulation. At [8], D.N. Katole, et.al proposed an improved SRF on the single-phase DVR series. With a depth of sag of V_S of 42%, this method produces a sag deviation of V_L of 7.6%. Furthermore, the FLC method for sag stress compensation was proposed by M.T. Hagh, et.al [10]. With a depth of sag of V_S of 92% without and 95% with DG, the FLC method yields a sag deviation of V_L of 8.9% without DG and 6.4% with DG, and a load THD_V of 1.26% without DG and 3.54 with DG. The SOGI-PLL method proposed by Yada et. Al [16], with a depth of sag of V_S of 30% was able to produce a sag deviation of V_L of 3.0%. S. Galeshi, et. al [17] already offer Multilevel Cascade H-Bridge Inverter topology. With a depth of sag of V_S of 20%, this topology produces a sag deviation of V_L of 0% and a load of THD_V of 4%. IDVR configuration with VSI and CSI has been proposed by R. Nittala, et.al [19]. With a depth of sag of V_S of 27.7% (with VSI and CSI), this configuration resulted in a sag deviation of V_L of 0%, load THD_V of 0.06% (with VSI) and 0.05% (with CSI). E. Babaei, et. al [22] have proposed a direct converter topology to mitigate voltage sag. With a depth of sag of V_S of 65%, this topology produces a sag deviation of V_L of 0% and a load THD_V of 7.07% (average).

The TDVR-PI configuration has been proposed by A. Benhail, et.al. [23]. With a depth sag of V_S, of 30%, this configuration results in a sag deviation of V_L of 2.18% and a load THD_V of 24%. J. Ye, et.al [26] have proposed an elliptical restoration method for voltage sag compensation and power factor correction. With a depth of sag of V_S, of 60%, this method is able to produce a source pf_{true} of 0.75 pu. The DVR-Super-capacitor configuration has been implemented by R. Omar, et.al [28]. With a depth of sag of V_S, of 30%, this topology is able to produce a sag deviation of V_L of 0 % and source THD_I of 2.38%. The CAESPDVR-ANFIS topology has been investigated by C.K. Sundarabalan, et. al. [29]. With a depth of sag of V_S, of 46.67% (average), this topology was able to produce a sag deviation of V_L of 0.4% and a load of THD_V of 2.35%. V.K. Awaar, et.al. [31] have implemented a VSI-SPWM-based single-phase DVR model with the NI-myRIO-1900 interface monitored in real-time by LabVIEW. With a depth of sag of V_S, of 50%, this model was able to produce a sag deviation of V_L of 8.79%. DVR control supplied by BES-PV using the UVTG method has been observed by A. Kiswantono [32]. With a depth of sag of V_S, of 80%, this configuration and method were able to produce a sag deviation of V_L of 2.89% (average) and a load THD_V of 5.81% (average). Based on the results of research [31] and [32], then this study has implemented the single-phase DVR model using the UVTG method with the Arduino-Uno interface monitored in real-time by LabVIEW. With a depth of sag of V_S of 80%, the proposed model is able to produce sag deviation of V_L of 6.4% (Bulb), 26.13% (FL), and 8.87% (LED). The model is also able to produce THD_I source of 1.523% (Bulb), 1.523% (FL), and 1.101% (LED) and pf_{true} respectively 0.985% (Bulb), 0.985% (FL), and 0.909% (LED). The proposed study is able to give the best performance because it is able to produce source THD_I lower than [28] and source pf_{true} is higher than [26]. Another contribution is that by using the Arduino-Uno interface, the proposed model can be run and monitored in real-time with LabVIEW. It is different from the simulations conducted by 12 previous researchers (except [31]) which were still carried out off-line using Matlab/Simulink environment.

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Reviewer comment to the authors:

6. Nobody can read the characters shown in Fig. 5. Enlarge or Redraw figure 5. You should use single column format for this figure.

Answer:

Thanks a lot for your valuable comment.

The answers to question number 6 are below:

a. I have enlarge Fig. 5 to help the reader see the characters shown in this figure (See Page 7 and Red Font).

b. I have use single column format for Fig. 5 (See Page 7 and Red Font).

c. I have added Fig. 5 with the explanation marked in red circles (A into G) to help the reader see and understand detail section of software design using LabVIEW interface for simulate signal. This sections are: (A) arduino-uno data communication, (B) source voltage (V_S), (C) injected voltage (V_{Inj}), (D) load voltage (V_{Inj}), (E) source current (I_S), (F) load current (I_L), (G) DC-link voltage ($V_{DC-Link}$), and (H) mixed signal graph (See Page 7 and Red Font).

Figure 5 before revised

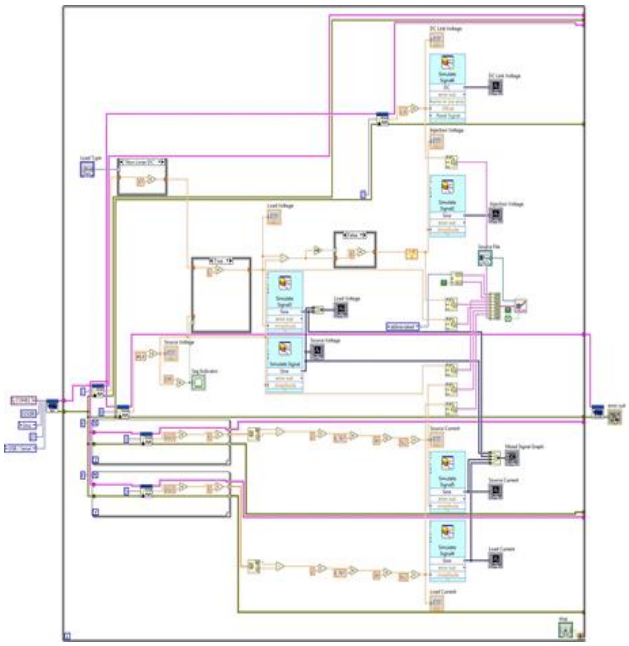

Fig. 5. Software design using LabVIEW interface

Figure 5 after revised

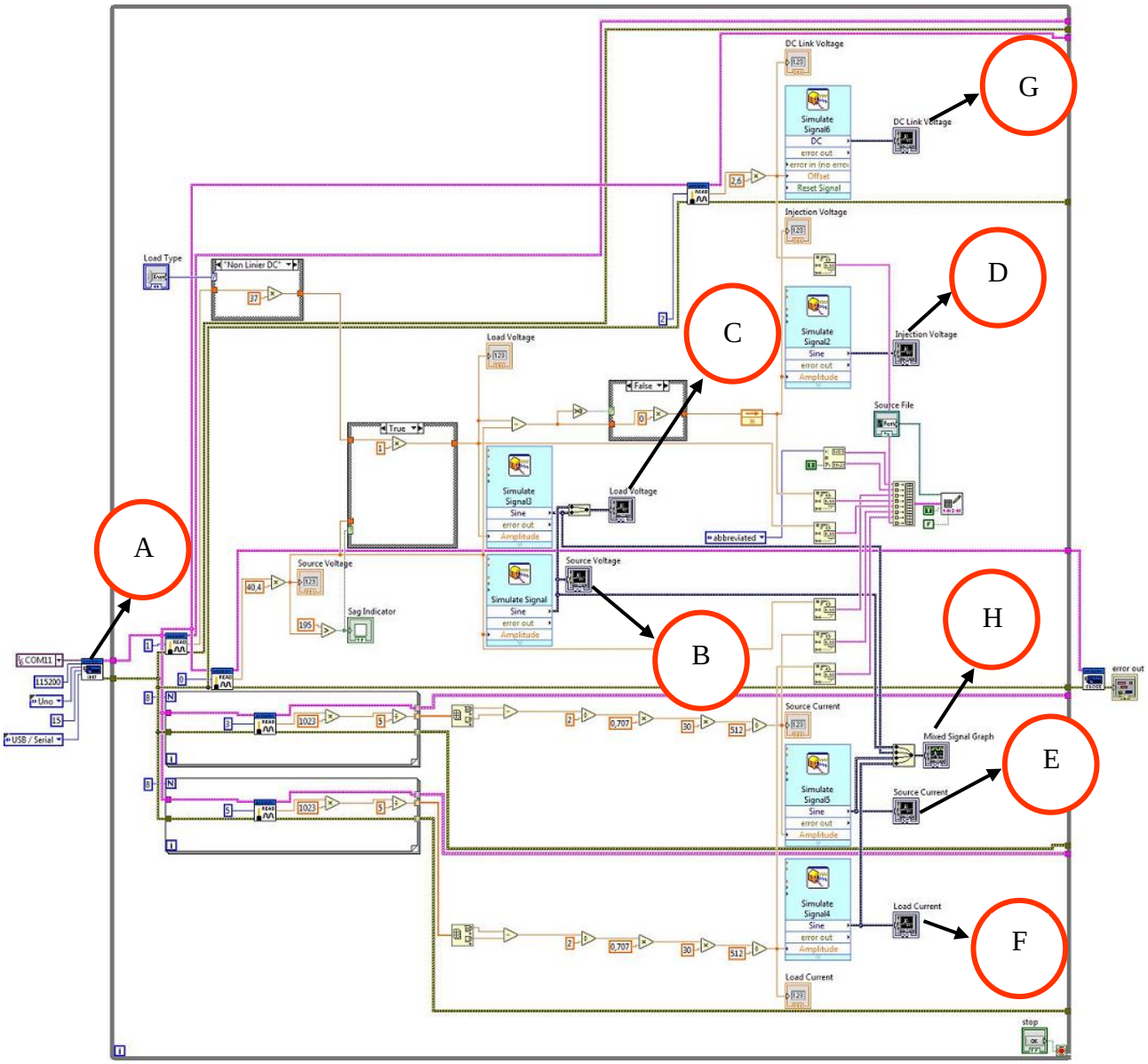

Figure. 5. Software design using LabVIEW interface for simulate signal i.e. (A) arduino-uno data communication, (B) source voltage (V_S), (C) injected voltage (V_{Inj}), (D) load voltage (V_{Inj}), (E) source current (I_S), (F) load current (I_L), (G) DC-link voltage ($V_{DC-Link}$), and (H) mixed signal graph

Reviewer comment to the authors:

7. The effectiveness of this work is not clear. Through simulations/experiments, the authors must justify the effectiveness of the proposed method by comparing with existing methods. Many articles are listed in references. However, no comparison is shown with these techniques. What's the meaning of References? Show comparison data.

Answer:

Thanks a lot for your valuable comment.

The answer to question number 7 is the same as the answer to question number 5.

Reviewer comment to the authors:

8. The results of this research are not clear in Conclusions. Furthermore, the benefits of the proposed method are not supported by theory. So, I fail to understand the scientific contribution of this research.

Answer:

Thanks a lot for your valuable comment.

8. The answers to question number 8 are below:
   a. The authors have added the contribution of this research at the end of the last paragraph 1 in the conclusion section ("……The proposed study is able to give the best performance because it is able to produce source THD_I lower than the previous studies. By using the Arduino-Uno interface, this model can be run and monitored in real-time with LabVIEW better from the simulations conducted by previous researchers which were still carried out off-line using Matlab/Simulink".) (See Page 12 and Red Font).
   b. The authors also have added the contribution of this research at the end of the last paragraph in the abstract section. (….."The proposed study is able to give the best performance because it is able to produce source THD_I lower than the previous studies. By using the Arduino-Uno interface, this model can be run and monitored in real-time with LabVIEW better from the simulations conducted by previous researchers which were still carried out off-line using Matlab/Simulink"). (See Page 1 and Red Font).
   c. The authors have discussed completely scientific contributions to this research on the answer to reviewer question number 5. (See Table 6 and its explanation on Page 11-12, Red Font)

Editor comment to the authors:

9. Please improve the reference format. This is very important for indexing service. If you did not follow the following format, your paper will be rejected automatically.

   *Do not use "et al." in author names.e.g.

   [1] R. Ruskone, S. Airault, and O. Jamet, "Vehicle Detection on Aerial Images", *International Journal of Intelligent Engineering and Systems*, Vol.1, No.1, pp.123-456, 2009. (In the case of Journal Papers)

   [2] R. Ruskone, L. Guigues, S. Airault, and O. Jamet, "Vehicle Detection on Aerial Images", In: *Proc. of International Conf. On Pattern Recognition*, Vienna, Austria, pp.900-904, 1996.

   (In the case of Conference Proceedings)

*Note: e.g. In the case of the author name:"John Doe", express as "J. Doe". ("John" is the first name and "Doe" is the family name.)

Answer:

Thanks a lot for your valuable comment.

9. The reference format has been improved below i.e.

Note: The revision is highlighted by red font

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[2] IEEE Std. 1159, "IEEE Recommended Practice for Monitoring Electric Power Quality", 1995.

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Editor comment to the authors:

10. Please add "Conflicts of Interest"(see the IJIES format.docx)

    Conflicts of Interest (Mandatory)

    Declare conflicts of interest or state "The authors declare no conflict of interest." Authors must identify and declare any personal circumstances or interest that may be perceived as inappropriately influencing the representation or interpretation of reported research results.

Answer:

Thanks a lot for your valuable comment.

10. Since submitting a paper for the first time, The authors have written "Conflict of Interest" in this paper section (See Page 13, Colomn 1, and Red Font).

Conflicts of Interest

The authors declare no conflict of interest.

Editor comment to the authors:

11. Please add "Author Contributions". (see the IJIES format.docx)

Author Contributions (Mandatory)

For research articles with several authors, a short paragraph specifying their individual contributions must be provided. The following statements should be used as follows: "conceptualization, XXX and YYY; methodology, XXX; software, XXX; validation, XXX, YYY, and ZZZ; formal analysis, XXX; investigation, XXX; resources, XXX; data curation, XXX; writing—original draft preparation, XXX; writing—review and editing, XXX; visualization, XXX; supervision, XXX; project administration, XXX; funding acquisition, YYY", etc. Authorship must be limited to those who have contributed substantially to the work reported.

Answer:

Thanks a lot for your valuable comment.

11. Since submitting a paper for the first time, The authors have written "Author Contributions" in this paper section (See Page 12-Colomn 1, Page 13-Column 1, and Red Font).

Author Contributions

Conceptualization, Y.A. Setiawan and A. Amirullah; methodology, Y.A. Setiawan and A. Amirullah; software, Y.A. Setiawan; validation, Y.A. Setiawan; formal analysis, Y.A. Setiawan and A. Amirullah; investigation, Y.A. Setiawan and A. Amirullah; resources, Y.A. Setiawan; data curation, Y.A. Setiawan; writing—original draft preparation, Y.A. Setiawan; writing—review and editing, Y.A. Setiawan; visualization, Y.A. Setiawan; supervision, A. Amirullah; project administration, Y.A. Setiawan; funding acquisition, A.Amirullah. All authors read and approved the final manuscript.

Adding Revision by the authors:

12. The authors have added reference [31] in this manuscript (…..[31] V.K. Awaar, P. Jugge, and T. Kalyani S, Optimal Design And Testing of A Dynamic Voltage Restorer For Voltage Sag Compensation And To Improve Power Quality, In: *Proc. of 42nd Annual Conference of the IEEE Industrial Electronics Society,* Florence, Italy, pp. 3745-3750, 2016) (See Page 14, Column 2, and Red Font). The authors also have mentioned this reference in introduction section (…..The DVR uses VSI method with SPWM to compensate for sag voltage has been implemented in [31]. The voltage sag was able to be simulated and monitored by LabVIEW with the NI myRIO-1900 interface using LabVIEW in real-time) (See Page 3, Column 1, and Red Font).
13. The author have added the future work in the last paragraph of conclusion section below: "……The measurement of source THD_V and load THD_V in the proposed model is also necessary to determine the harmonic mitigation performance of the voltage within the IEEE 519 limit". (See Page 12, Column 2, Paragraph 2 on Conclusion Section, Red Font).
14. The author have revised Fig. 3-A schematic diagram of single phase DVR-BES, below: (See Page 5, Column 2).

Figure. 4 Before Revised

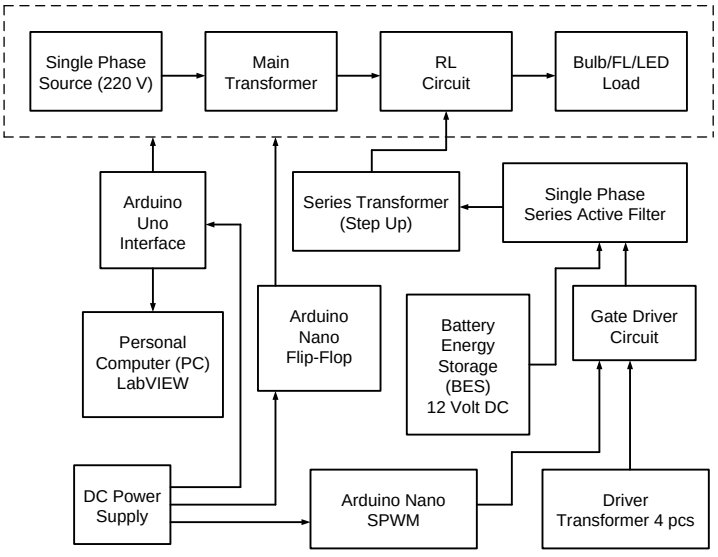

Fig. 3. A schematic diagram of single phase DVR-BES

Figure. 4 After Revised

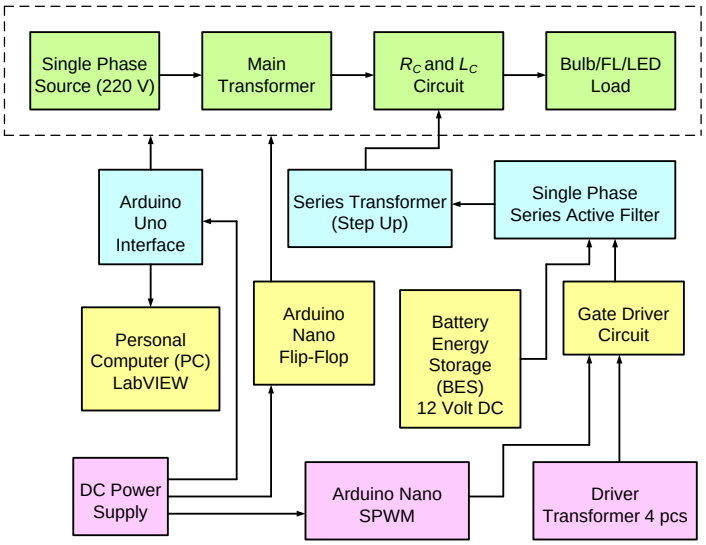

Figure. 3 A schematic diagram of single phase DVR-BES

15. The author have revised Figure. 4 Single-phase DVR-BES below (See Page 6, Column 2).

Figure. 4 Before Revised

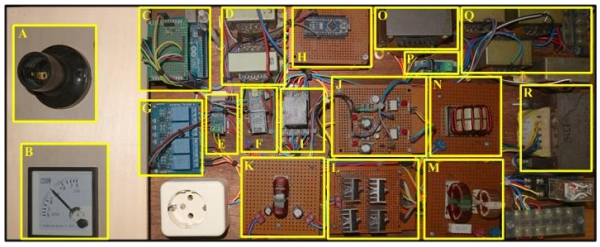

Figure. 4 Single-phase DVR-BES hardware

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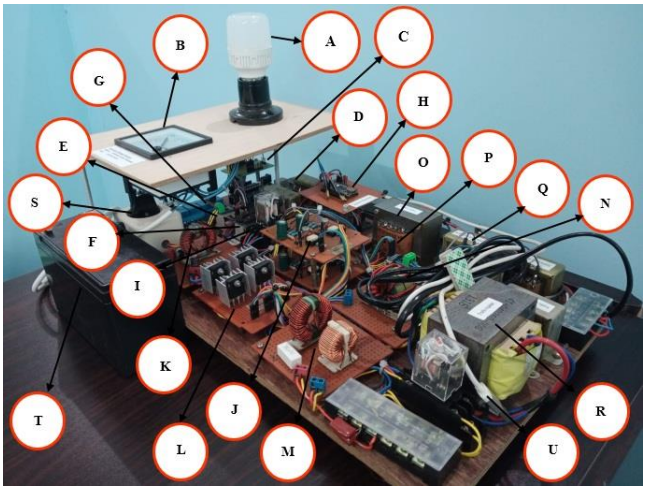

Figure. 4 Single-phase DVR-BES hardware

**) For Reviewer 1, Reviewer 2, and Editor:

1. Thanks a lot for your constructive comments.
2. We are appreciate for your kind guidance and valuable advices.

Lampiran 2.5

Hasil Revisi Makalah

Submitted

Received: October 18, 2020. Revised: December 20, 2020.

INASS

International Journal of
Intelligent Engineering & Systems

http://www.inass.org/

Implementation of Single-Phase DVR-BES Based on Unit Vector Template Generation (UVTG) to Mitigate Voltage Sag Using Arduino Uno and Monitored in Real-Time Through LabVIEW Simulation

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Abstract: This paper aims to design and implement a single-phase dynamic voltage restorer (DVR) supplied by battery energy storage (BES) using load voltage controlled by the unit vector template generation (UVTG) method. The UVTG method on the DVR system is implemented using the Arduino-Uno hardware. LabVIEW-based interface simulation is used for monitoring the parameter in real-time during 80% voltage sag period i.e. source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power factor measurements are also carried out to obtain total harmonic distortion (THD) of the source current and load current. The single-phase DVR system is connected to load i.e. a 5-watt bulb lamp (linear-load), 5-watt fluorescent (FL) lamp (non-linear load), and 5-watt light-emitting diode (LED) lamp (non-linear load). During voltage sag, the single-phase DVR-BES system is able to maintain load voltage i.e. bulb lamp, FL lamp, and LED lamp of 216 volts, 256 volts, and 185 volts, respectively. The percentage of load sag voltage deviation for each load is 6.4%, 26.13%, and 8.87%, respectively. The measurement of source power-factor with voltage sag results in source true power factor of three loads of 0.985 pu leading, 0.985 pu leading, and 0.990 pu leading respectively. On the same system with voltage sag, single phase DVR-BES is able to result in source current harmonics (THD_I) for three loads of 1.523%, 1.523%, and 1.010% respectively. The proposed study is able to give the best performance because it is able to produce source THD_I lower than the previous studies. By using the Arduino-Uno interface, this model can be run and monitored in real-time with LabVIEW better from the simulations conducted by previous researchers which were still carried out off-line using Matlab/Simulink.

Keywords: Single Phase DVR, BES, Arduino Uno, LabVIEW, Voltage Sag

1. Introduction

During the last decade, there has been an increase in the number of sensitive and critical loads. On the other hand, the use of these tools also has an impact on deteriorating Power Quality (PQ). Among a number of PQ problems, problems related to voltage mitigation are also of increasing importance from a sensitive load and customer point of view. PQ problems related to voltage i.e. voltage sag, voltage swell, voltage harmonics, fluctuations, interruptions, and imbalance. In accordance with IEEE 1346 [1] and IEEE 1159 [2] standards, the sag voltage is defined as the RMS (root mean square) AC voltage sag with a magnitude of 10% to 90% of the nominal voltage, at power frequencies with a duration of 0.5 cycles to one minute. The voltage sag is caused by a single-phase short circuit to ground in the power system, starting in large-capacity induction motors, and sudden changes in the system connected to large loads [3]. Viewed from the system, the DVR is divided into two systems, namely one-phase DVR and three-phase DVR. Then three-phase DVR is connected to a 3 phase 3 wire (3P3W) or a 3 phase 4 wire (3P4W) system. Next, this paper will further focus on the design and implementation of single-phase DVRs to mitigate voltage sag at the source side and connect to a number of the linear/non-linear load. The simulation of low voltage single phase DVR based on the multilevel

inverter to protect sensitive loads has been implemented in [4]. The proposed model is able to compensate for the voltage sag and increase the PQ on the load side. A DVR topology using a cascaded multilevel direct pulse with modulation (PWM) ac-ac converter has been proposed in [5]. In this scheme, the unit cell of the multilevel converter consists of a single-phase ac-ac converter PWM using a switching cell (SC) structure that is paired with an inductor. The implementation of the phase shift PWM technique is capable of significantly reducing the size of the output filter inductor. One and three-phase DVR control schemes using PSCAD/EMTDC have been observed in [6]. The proposed system is able to compensate for a number of voltage sag variations and keep the load voltage constant. DVR control scheme with an ac-ac converter, based on voltage drop characterization has been investigated in [7] to reduce voltage drop with phase jumps. The superiority of the proposed control scheme is then validated on an ac-ac interphase converter topology. The vector-based one-phase DVR control using an improved synchronous reference frame (SRF) has been proposed in [8]. The vector analysis used in this control method during the voltage period was able to provide the magnitude and phase of the injection voltage.

The control methods to reduce sag voltages using a fuzzy logic controller (FLC) connected with sensitive loads [9] and distributed generation (DG) [10] have been proposed. The FLC control was used to generate pulses with the Sinusoidal Pulse Width Modulation (SPWM) technique at the output of an active filter circuit. Comparing to proportional-integral (PI) control, FLC control was able to provide better performance during voltage sag because it has more advantages in terms of resistance to parameter variations and system execution. A DVR with DG-connected FLC control also able to enhance voltage profiles, power quality, and reliability. Single-phase and three-phase DVRs use a single-phase ac to ac matrix converter to replace voltage source inverter (VSI), has been investigated by Matlab in [11],[12], and in PSCAD [13], at a number of variations in source voltage (sag, flicker, and unbalance). The single-phase DVR has been simulated in [14] and a special voltage detection method for single-phase DVRs has been introduced in [15]. The simulation results show that the DVR was able to maintain the nominal load voltage, despite interference and other abnormal conditions from the source side. The special detection method using double closed-loops of the proportional-resonant controller was also able to provide superior performance in voltage detection and compensation.

The DVR control scheme for reference voltage generation based on a single-phase Second Order Generalized Integrator-Phase Lock Loop (SOGI-PLL) using a series of active compensator has been observed in [16]. The proposed scheme is capable of dynamically responding, detecting, and rapidly compensating for sag/swell voltages without and with phase jumps. A DVR that uses a multilevel H-bridge inverter with a capacitor as an energy source has been introduced in [17]. This configuration allows the DVR to connect directly to a medium-voltage network, eliminating the need for a series injection transformer and batteries. The DVR model was the same but uses a single H-Bridge inverter and a battery on sag/swell voltage disturbances connected to the non-linear load which has also been observed in [18]. Interline DVR (IDVR) on two same [19] and different voltage distribution lines with voltage source inverter (VSI) and current source inverter (CSI) [20] to restore voltage sag and harmonics has been introduced. When voltage sag and voltage distortion occur on one channel, the DVR on the same channel is able to perform voltage compensation and harmonics elimination, while the other DVR can recharge the energy to the DC-link to maintain the DC-link voltage constant.

In order to efficiently the number of equipment in the DVR circuit configuration, the implementation of a direct ac/ac converter on the DVR has been introduced in [21],[22]. The proposed configuration uses the minimum switches, did not require a dc-link energy storage element, and has a longer compensation time during sag/swell voltage disturbances. The compensation voltage for each phase is taken from each of the three-phase sources so that each converter was able to operate independently and is also able to compensate for single-phase blackouts and unbalance sag/swell voltages. The use of a single-phase transformer-less DVR (TDVR) to mitigate the sag/swell voltage has been observed in [23]. The proposed configuration was capable of reducing system size and losses compared to DVR which using a series transformer. The single-phase interactive channel DVR using the sag voltage detection algorithm has been developed in [24]. The detection algorithm has a hybrid structure consisting of a momentary detection section and a RMS variation detection section. The DVR development could compensate for input voltage sag or interrupt in 2.0-ms delay and can be used effectively for sensitive loads.

The single-phase DVR with synchronous reference frame control under distorted source conditions has been applied in [25]. The proposed control using a moving average filter (MAF) is capable of extracting positive sequence fundamental components as well as being able to mitigate voltages sag and distorted source voltages. The single-phase DVR using elliptical restoration-based voltage compensation to correct the power factor on the source side has been proposed in [26]. The active and

reactive voltage components and centrifugal angles are used to formulate an elliptical compensation path. So that the voltage will be in-phase with the load current using precise control of the DVR injection voltage. The optimization of the voltage injection technique in DVR to protect sensitive loads has been observed in [27]. The recursive least square (RLS) method is used to estimate the magnitude and phase of the voltage in order to minimize the amplitude of the injection voltage. Meanwhile, repetitive control was proposed to track the compensation voltage. Both controls are suitable for sinusoidal reference and are reliable for mitigating harmonics, sags, and swell distortions.

Energy storage in single or three-phase DVR circuits related to the capacity and type of energy storage has become the attention of many researchers. The determination of the two parameters relates to the ability and duration of the energy storage to supply real power to the inverter during a fault. Unbalanced voltage compensation in 3P3W system using DVR using a super capacitor has been investigated in [28]. The proposed DVR configuration uses a control based on the d-q-0 and Proportional Integral (PI) transformation technique and is further coded using a digital signal processor (DSP). DSP control and super capacitor implementation can mitigate unbalanced voltage disturbances. A compressed air energy storage powered dynamic voltage restorer (CAESPDVR) with ANFIS control has been proposed in [29] to compensate for unbalanced sag/swell voltages and harmonics. The single-phase DVR configuration using a hybrid energy storage system (HES) has been developed in [30].

The HES series consists of superconducting magnetic energy storage (SMES) in collaboration with battery energy storage (BES) on a DC type DVR. The proposed HES concept integrated with fast response large power SMES unit and low-cost high capacity BES can further be implemented in large scale DVR development. The DVR uses VSI method with SPWM to compensate for sag voltage has been implemented in [31]. The voltage sag was able to be simulated and monitored by LabVIEW with the NI myRIO-1900 interface using LabVIEW in real-time. The mitigation of sag/swell voltage and harmonics in low voltage distribution networks using DVR-BES-PV using the UVTG control method has been observed in [32]. The proposed model was able to compensate for sag voltage between 10% to 90% and swell voltage between 110% to 180% with a voltage THD within the IEEE 519 limit.

In this paper, BES is proposed as energy storage and implemented in single-phase DVR using load voltage control with the UVTG method and connected to linear/non-linear loads. The UVTG method on the DVR system is implemented using the Arduino-Uno microcontroller hardware. The LabVIEW based interface simulation is used to monitor electrical quantities in real-time during the voltage sag period i.e. source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power factor measurements are also carried out to obtain the total harmonic value or Total Harmonic Distortion (THD) of the source current and load current.

This paper is arranged as follows. Section 2 presents the proposed method, UVTG method, percentage of voltage sag, true power factor and harmonic, single-phase DVR-BES using LabVIEW, as well as hardware and software implementation, Section 3 presents results and discussion of the source voltage, injection voltage, load voltage, DC-link voltage, source current, load current, percentage of voltage sag, true power-factor, and current THD which analyzed from data measured by Arduino-Uno and monitored by LabVIEW. In this section, the system connected to the linear/non-linear load with and without voltage sag is selected to present the best performance single-phase DVR-BES system connected to three different types of load during voltage sag. Finally, this paper is concluded in Section 4.All manuscripts must be in English. These guidelines include complete descriptions of the fonts, spacing, and related information for producing your proceedings manuscripts. Table 1 shows the abbreviations used in this paper.

Table 1. Abbreviation

Symbol	Description
PQ	Power Quality
DVR	Dynamic Voltage Restorer
BES	Battery Energy Storage
PV	Photovoltaic
UVTG	Unit Vector Template Generation
THD	Total Harmonic Distortion
Pf_{true}	True Power Factor
FL	Fluorescent
LED	Light Emitting Diode
DG	Distributed Generation
3P3W	Three Phase Three Wire
3P4W	Three Phase Four Wire
SPWM	Sinusoidal Pulse Width Modulation
VSI	Voltage Source Inverter
CSI	Current Source Inverter
SOGI-PLL	Second Order Generalized Integrator-Phase Lock Loop
CAESPDVR	Compressed Air Energy Storage Powered Dynamic Voltage Restorer
ANFIS	Artificial Intelligent Fuzzy Inference System
IDVR	Interline Dynamic Voltage Restorer
CB	Circuit Breaker
RMS	Root Mean Square
GUI	Graphic User Interface
PC	Personal Computer
USB	Universal Serial Bus
PU	Per Unit

2. Research Method

2.1. Proposed Method

Fig. 1 shows a single-phase DVR supplied by BES using load voltage control with the UVTG method. The DVR is a tool that functions to compensate for the load voltage in the event of a voltage sag disturbance on the source bus at a level of 0.1 to 0.9 per unit. The UVTG method on the DVR system is implemented using the Arduino-Uno hardware. LabVIEW-based interface simulation is used to monitor electrical quantities in real-time during the voltage sag period.

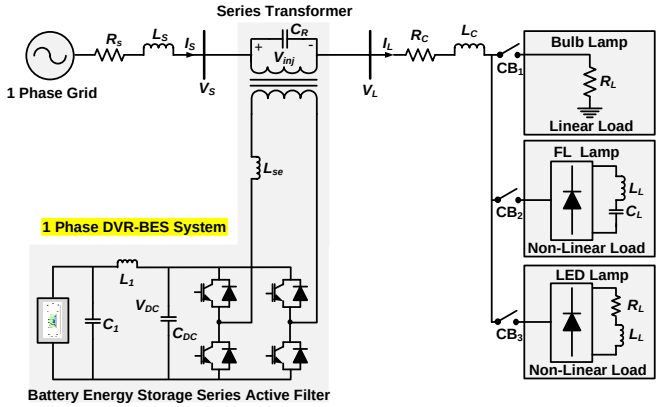

Figure. 1 Proposed single phase DVR-BES connected to linear/non-linear load

The observed parameters are source voltage (V_S), injection voltage (V_{inj}), load voltage (V_L), DC-link voltage ($V_{DC-Link}$), source current (I_S), and load current (I_L). The true power-factor (Pf_{true}) measurements are also carried out to obtain the THD value of the source current and load current. There are two cases in this study, the source without voltage sag, and with an 80% voltage sag. In each case, the single-phase DVR system is supplied by BES connected to a 5-watt bulb lamp (linear load), 5 watt FL lamp (non-linear load), and 5 watts LED lamp (non-linear load), so the total selected case is six. The CB1, CB2, and CB3 are used to connect and disconnect links to three linear/non-linear loads. The DVR-BES system configuration is then run based on a predetermined case using Arduino-Uno microcontroller interfaced communication and the results are simulated and monitored in real-time by a LabVIEW. Table 2 shows the notation list and parameters of Fig. 1.

Table 2. Notation list and parameters

Notation	Description
V_S	Source Voltage
V_{inj}	Injection Voltage
V_L	Load Voltage
$V_{DC-Link}$	DC-Link Voltage
I_S	Source Current
I_L	Load Current
I_L^*	Reference Load Voltage
V_m	Peak Fundamental Input Voltage Magnitude
K	Gain
S_1, S_2, S_3, S_4	Gating Signal 1, 2, 3, and 4
Sag_{dev}	Voltage Sag Deviation
$V_{pre-sag}$	Pre-Sag Voltage
V_{sag}	Sag Voltage
Pf_{true}	True Power Factor
P_{avg}	Average Power
S	Apparent Power
V_{rms}	RMS Voltage
I_{rms}	RMS Current
V_{1rms}	RMS Fundamental Voltage
I_{1rms}	RMS Fundamental Current
THD_V	Voltage THD
THD_I	Current THD
P_{1avg}	Fundamental Average Power
$Pf_{displacement}$	Displacement Power Factor
$Pf_{distorted}$	Distorted Power Factor
R_S	Line Resistance (0.1 ohm)
L_S	Line Inductance (0.15 mH)
R_C	Load Resistance (0.4 ohm)
L_C	Load Inductance (15 mH)
L_{Se}	Series Inductance (0.015 mH)
L_1	BES Inductance (6 mH)
C_1	BES Capacitance (1000 µF)
C_{DC}	DC-Link Capacitance (200 µF)
R_L	Linier/Non-Linear Resistance (0.6 ohm)
L_L	Non-Linear Load Inductance (0.15 mH)
C_L	Non-Linear Load Capacitance (3.3 µF)
C_R	Ripple Capacitance (0.2 µF)

2.2. Unit Voltage Template Generation Method

The series active filter protect sensitive loads against several voltage disturbances from the source bus. In [31], the control method of source and load voltage in a three-phase series active filter has been discussed. Using the same procedure, the authors propose the same method for single-phase series active filter control as shown in Fig. 2. This method extracts UVTG from the distorted input supply. Then, the template is expected to be an ideal sinusoidal signal with a unity amplitude. The source of the distorted voltage is measured and divided by the peak amplitude fundamental input voltage (V_m).

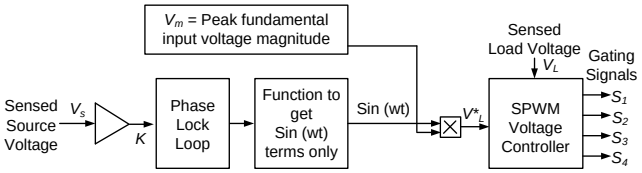

Figure. 2 UVTG control on single phase series active filter

A single-phase locked loop (PLL) is used in order to generate sinusoidal unit vector templates with a phase lagging by the use of the sine equation. The

reference signal of the load voltage is calculated by multiplying the unit vector templates with the peak amplitude of the fundamental input voltage (V_m). The reference load voltage (V_L^*) is then compared to the sensed load voltage (V_L) by a SPWM controller used to generate the desired four gating signal on a single-phase series active filter.

2.3. Percentage of Voltage Sag Deviation

The recommended standard of practice on monitoring voltage sag/swell as part of electric power quality parameters is IEEE 1159 [2]. This standard presents the definition and table of voltage sag base on categories (instantaneous, momentary, temporary) typical duration, and typical magnitude. The percentage of load voltage sag deviation is formulated in Eq. (1) [31].

$$Sag_{dev}(\%) = \frac{|Vpre\_sag - V\_sag|}{Vpre\_sag} \quad (1)$$

2.4. True Power Factor and Harmonics

The true power factor at the load is defined as the ratio of average power to apparent power. The true power factor for both sinusoidal and non-sinusoidal situations is presented in Eq. (2) [33].

$$pf_{true} = \frac{P_{avg}}{S} = \frac{P_{avg}}{V_{rms}\, I_{rms}} \quad (2)$$

$$V_{rms} = V_{1rms}\sqrt{1 + (THD_V/100)^2} \quad (3)$$

$$I_{rms} = I_{1rms}\sqrt{1 + (THD_I/100)^2} \quad (4)$$

By substituting Eq. (3) and Eq. (4) into Eq. (2), the true power factor (Pf_{true}) results in Eq. (5) for both sinusoidal and non-sinusoidal cases [33].

$$pf_{true} = \frac{P_{avg}}{V_{1rms}\, I_{1rms}\sqrt{1+(THD_V/100)^2}\sqrt{1+(THD_I/100)^2}} \quad (5)$$

A useful simplification can be made by expressing Eq. (5) as a product of two components defined in Eq. (6).

$$pf_{true} = \frac{P_{avg}}{V_{1rms}\, I_{1rms}} \times \ldots\ldots \frac{1}{\sqrt{1+(THD_V/100)^2}\sqrt{1+(THD_I/100)^2}} \quad (6)$$

By making the following two assumptions: (1) In most cases, the contributions of harmonics above the fundamental to average power are very small, so that is $P_{avg} \approx P_{1avg}$ and (2) Since THD_V is less than 10%, then from (12) we see that $V_{rms} \approx V_{1rms}$. Then, merging both assumptions into Eq. (6) results in the following approximate function for the true power factor (Pf_{true}) presented in Eq. (7) [33].

$$pf_{true} = \frac{P_{1avg}}{V_{1rms}\, I_{1rms}} \times \frac{1}{\sqrt{1+(THD_I/100)^2}} = Pf_{displacement} \times Pf_{distorted} \quad (7)$$

Because displacement power factor (Pf_{disp}) could never be greater than unity, Eq. (7) shows that the true power factor (Pf_{true}) in non-sinusoidal cases has the upper limit so finally its function is defined in Eq. (8) [33].

$$pf_{true} \le Pf_{distorted} = \frac{1}{\sqrt{1+(THD_I/100)^2}} \quad (8)$$

2.5. Single Phase DVR-BES using LabVIEW

The implementation of the single-phase DVR-BES system consists of several stages. That stage i.e. create a single-phase series active filter, create a gate driver to trigger the MOSFET in the series active filter, create a SPWM program to drive the gate driver as an inverter trigger and create a monitoring program in LabVIEW. Fig. 3 presents a schematic diagram of a single phase DVR-BES system.

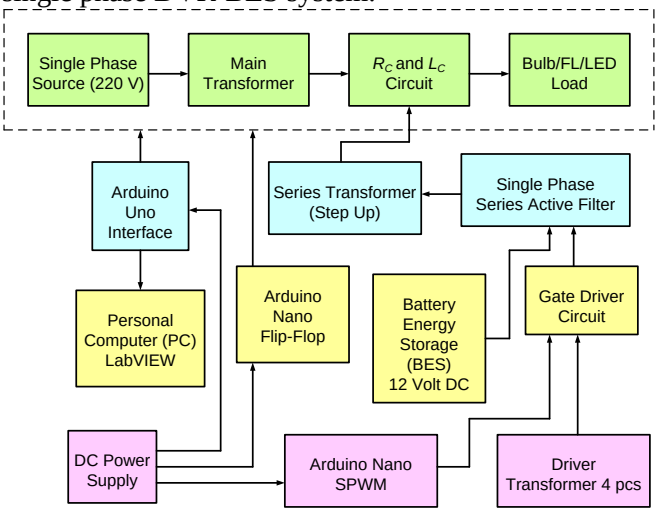

Figure. 3 A schematic diagram of single phase DVR-BES

Fig. 3 shows that the BES and series active filters play an important role in compensating for the voltage sag on a single-phase DVR. The step-up transformer that is installed in a series against the load functions to inject the voltage from the series active filter to the load. The main energy source for series active filters uses BES DC voltage 12 V with a capacity of 7.2 Ah. The process of changing the DC to AC voltage begins with the Arduino Nano SPWM microcontroller providing Sinusoidal SPWM pulses to the Gate Driver circuit which has the main component of the TLP 250 Optocoupler IC, then the Gate Driver circuit triggers the IRFP250 MOSFET gate on a series active filter circuit cross-like as an electric current cycle in the circuit bridge diode rectifier. So that it will produce an AC output from a series active filter circuit. The output voltage of the series active filter is an AC

voltage of 7 V depending on the battery voltage conditions, which will then be increased to an AC voltage of 220 V using a step-up transformer. The step-up series transformer has a power of 600 VA with a primary AC input voltage of 7.2 V and a secondary AC output voltage of 220 V. The goal is that the series active filter is able to inject enough power to compensate for the sag voltage at a level of 10% to 90%.

The Arduino Nano flip-flop functions as a timer to run system simulations using a single-phase DVR-BES without and with sag voltage. The Arduino nano has been programmed with a flip-flop program with the 1-second case instructing the relay to turn "on" as a representation of the system experiencing sag voltage and 1 second ordering the relay to turn "off" as a representation of the system without experiencing sag voltage. This timer is expected to function when there is a sag voltage and automatically orders a single-phase active filter to inject a voltage compensation into the load so that the load voltage will remain stable.

The Arduino Uno interface functions as a medium for receiving data from voltage sensors and current sensors that are measuring the amount of electricity in the DVR circuit and sending the data to a personal computer (PC) with LabVIEW software. Curves and data displayed in LabVIEW i.e. source voltage, load voltage, injection voltage, DC-link voltage, source current, and load current respectively. The display form implemented in LabVIEW is in the form of graphs and number indicators. With a graphic display, the reader will find it easier to observe the wave condition both voltage and current during the system condition without and with voltage sag. All data displayed in LabVIEW is real-time and continuous data as long as the single-phase DVR-BES system is operated to the system. In addition to using the LabVIEW, data collection is also carried out by the cos-phi meter to determine the value of the true power factor of source and load as a basis for determining the harmonic of source and load currents. The single-phase DVR-BES system connected to three linear/non-linear loads i.e. bulb lamp 5 W (linear), FL lamp 5 W (non-linear), LED lamp 5 W (non-linear) respectively.

2.6. Hardware and Software Implementation

The LabVIEW interface software diagram consists of the main program in the form of a Graphic User Interface (GUI) which functions to run all indicators and controls on the front panel. Fig. 4 shows the model of the single-phase DVR-BES hardware circuit. The nominal parameters of Fig. 4 are presented in Table 3.

Table 3. Nominal of device parameters

Devices	Design Values
Single phase source voltage	220 V
Frequency	50 Hz
Series Transformer (*step-up)*	600 VA 7,2/220 V
Main Transformer (CT)	3 A
Current Sensor ACS 712	5A
Relay	1 device
Arduino Uno (Interface)	1 device
Arduino Nano (Flip-Flop)	1 device
Arduino Nano (SPWM))	1 device
Load Resistance (R_C)	0.4 ohm
Load Inductance (L_C)	15 mH
Cos-phi-Meter	1 device
Battery Energy Storage (BES)	12 V/7.2 Ah
DC-link Capacitance (C_{DC})	1000 μF
Bulb Lamp Load	5 W
FL Lamp Load	5 W
LED Lamp Load	5 W

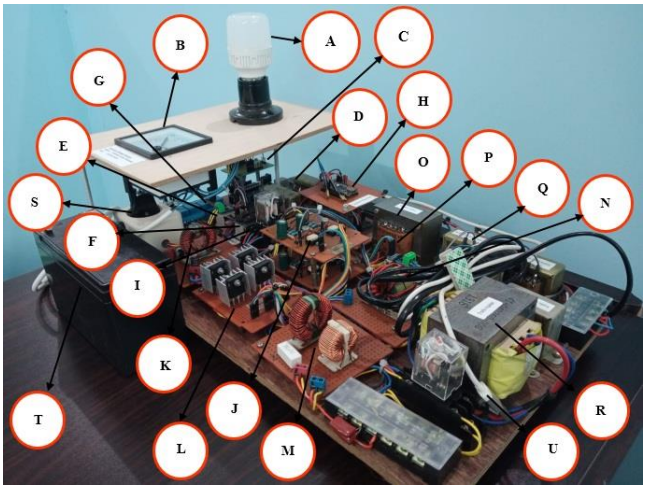

Figure. 4 Single-phase DVR-BES hardware

Where A: Load; B: Cos-phi-meter; C: Arduino Uno; D: Voltage Sensor Transformer; E: Current Sensor; F: Arduino Nano SPWM; G: Relay 1 (4 Channel); H: Arduino Nano Flip-Flop; I: Two Relays (220V-AC); J: Gate Driver Optocoupler; K: DC-link Capacitance and BES filter (C_{DC}, L_1, C_1); L: Series Active Filter; M: Load Impedance (R_C, L_C); N: Series Inductance (L_{Se}); O: Main Transformer; P: Source Current Sensor; Q: Gate Driver Transformer; R: Series Transformer; S: Source Voltage; T: BES and U: Universal Serial Bus (USB) for data communication between hardware PC.

Fig. 5 shows the overall GUI program design and the component parts of the single-phase DVR-BES. In order for the LabVIEW software interface on the PC to communicate with the Arduino Uno, a program is needed to communicate the two devices. The communication program used by Lifa Base. Lifa Base is the driver for Arduino Uno in connecting data communication with PC. Lifa Base is the default program from Arduino when users install LabVIEW.

3. Results and Discussion

Fig. 1 shows a series of DVR supplied by BES connected to a load of Bulb, FL, and LED respectively. The series transformer connected to the load functions to inject the voltage from the series active filter during voltage sag. The Arduino Nano Flip-Flop is used as a timer to run simulated data collection. The cycle timer applied to the DVR is 1 second on and 1 second off. The data collection period is carried out with a LabVIEW simulation for 3 seconds, with 80% depth of source voltage sag duration between 1 to 2 seconds. Data collection is carried out at 1.5 seconds from the curve of the source voltage (V_S), injection voltage (V_{inj}), load voltage (V_L), DC-link voltage ($V_{DC-Link}$), source current (I_S), and load current (I_L), curves. The true power-factor (Pf_{true}) data in the source bus and load bus is measured from the cos-phi meter.

Using the same LabVIEW simulation procedure and period, data collection is also carried out without the voltage sag. The percentage of load voltage sag deviation is calculated using Eq. (1) with a pre-sag voltage of 203 V. Base on true power-factor, then harmonics current is measured using Eq. (8). Table 4 presents the performance of voltage, current, and percentage of sag deviation of load voltage (V_L) of the single-phase DVR supplied by BES without and with voltage sag disturbance. Table 5 presents the performance of true power factor (Pf_{true}) and harmonics value of the single-phase DVR supplied by BES without and with voltage sag disturbance. Fig. 6, Fig. 7, and Fig. 8 show the performance of voltage and current of the single-phase DVR supplied by BES connecting to bulb lamp, FL lamp, and LED lamp load respectively.

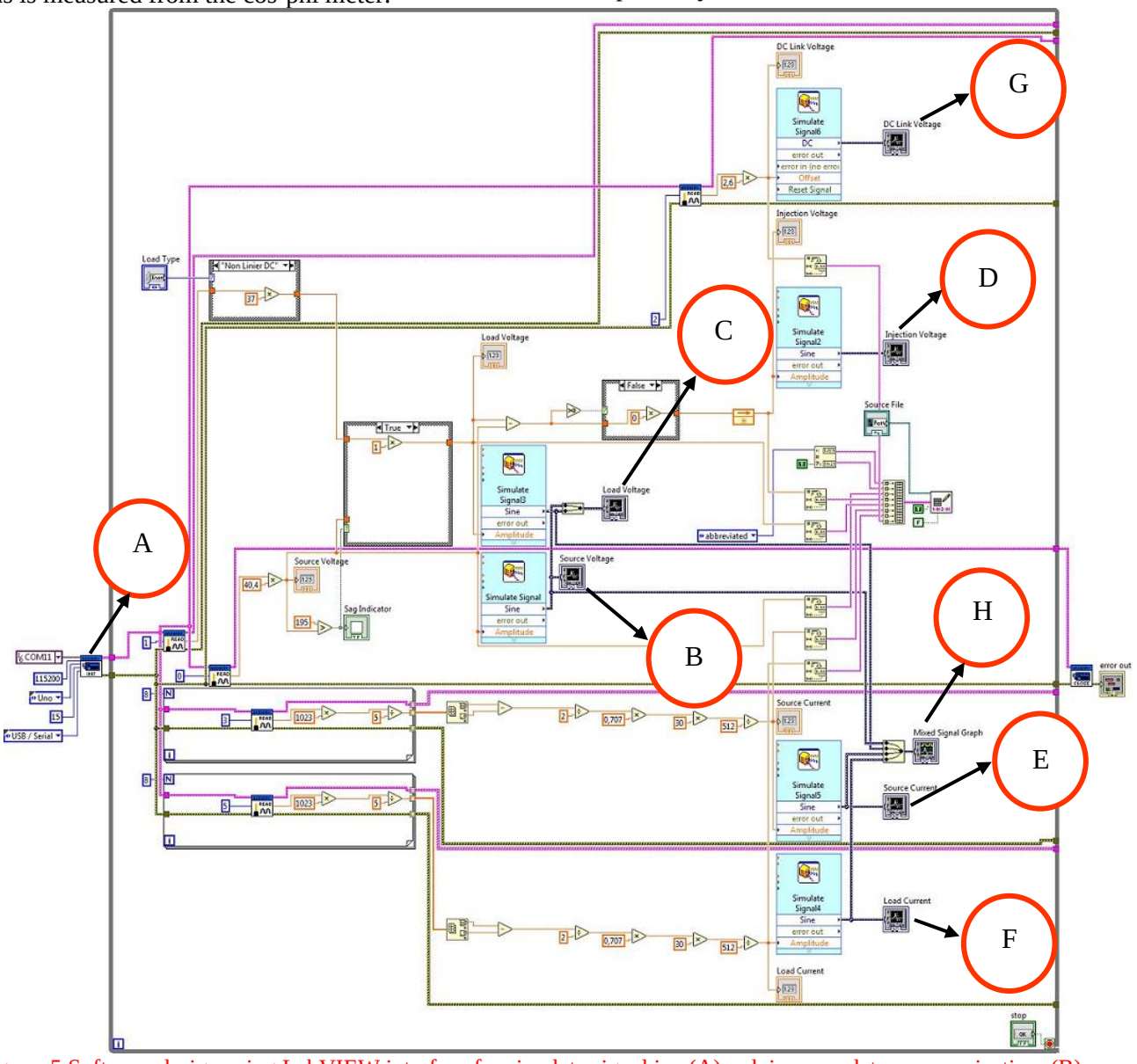

Figure. 5 Software design using LabVIEW interface for simulate signal i.e. (A) arduino-uno data communication, (B) source voltage (V_S), (C) injected voltage (V_{Inj}), (D) load voltage (V_{Inj}), (E) source current (I_S), (F) load current (I_L), (G) DC-link voltage ($V_{DC-Link}$), and (H) mixed signal graph

Table 4. Performance of voltage, current, and sag deviation of load voltage of the single-phase DVR supplied by BES

No.	Load Type	V_S (V)	$V_{Inj}(V)$	V_L (V)	I_S (A)	I_L (A)	$V_{DC-Link}$ (V)	Sag Dev of V_L (%)
Without Voltage Sag								
1.	Bulb Lamp	203	0	203	0.208	0.166	13.03	0
2.	FL Lamp	203	0	203	0.208	0.083	13.03	0
3.	LED Lamp	203	0	203	0.270	0.166	13.03	0
With Sag Voltage								
4.	Bulb Lamp	44.7	168	216	0.228	0.145	8.20	6.40
5.	FL Lamp	50.3	200	256	0.166	0.208	7.33	26.13
6.	LED Lamp	49.1	133	185	0.249	0.789	8.06	8.87

Table 5. Performance of power factor and harmonics of the single-phase DVR supplied by BES

No.	Load Type	Source Pf_{true} (pu)	Load Pf_{true} (pu)	Source THD_I (%)	Load THD_I (%)
Without Voltage Sag					
1.	Bulb Lamp	0.850	0.999	17.647	0.1001
2.	FL Lamp	0.900	0.999	11.111	0.1001
3.	LED Lamp	0.990	0.999	1.010	0.1001
With Sag Voltage					
4.	Bulb Lamp	0.985	0.998	1.523	0.2040
5.	FL Lamp	0.985	0.998	1.523	0.6040
6.	LED Lamp	0.990	0.975	1.010	2.5640

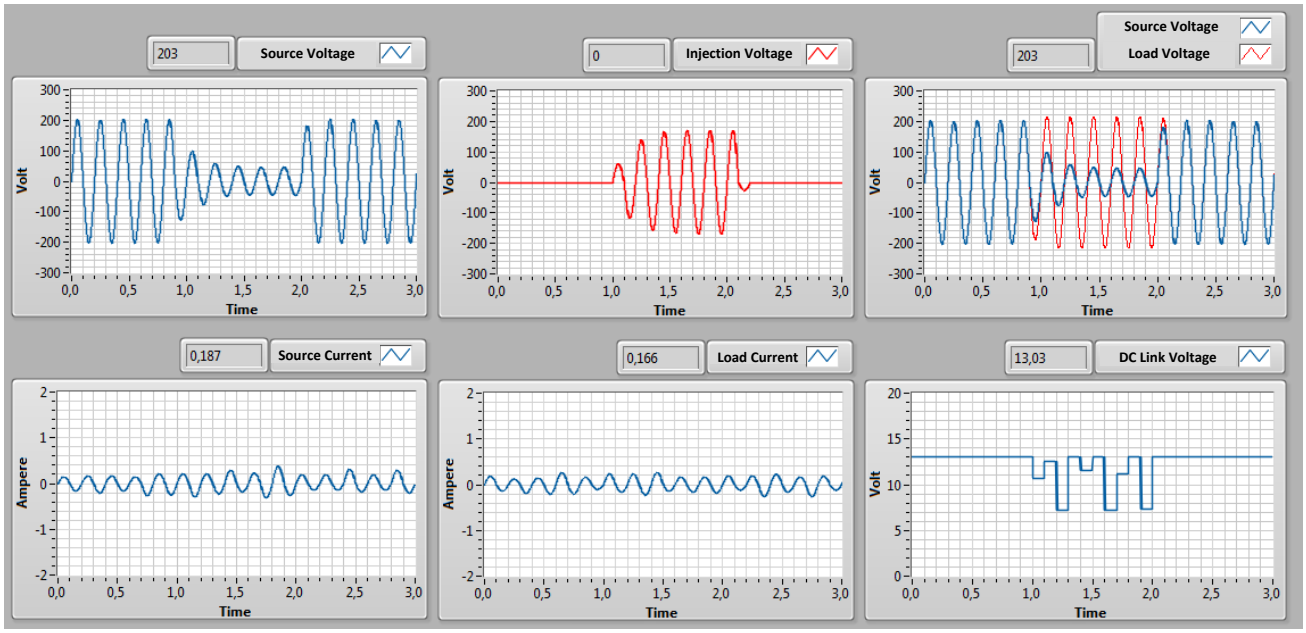

Figure. 6 Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to bulb lamp load using LabVIEW

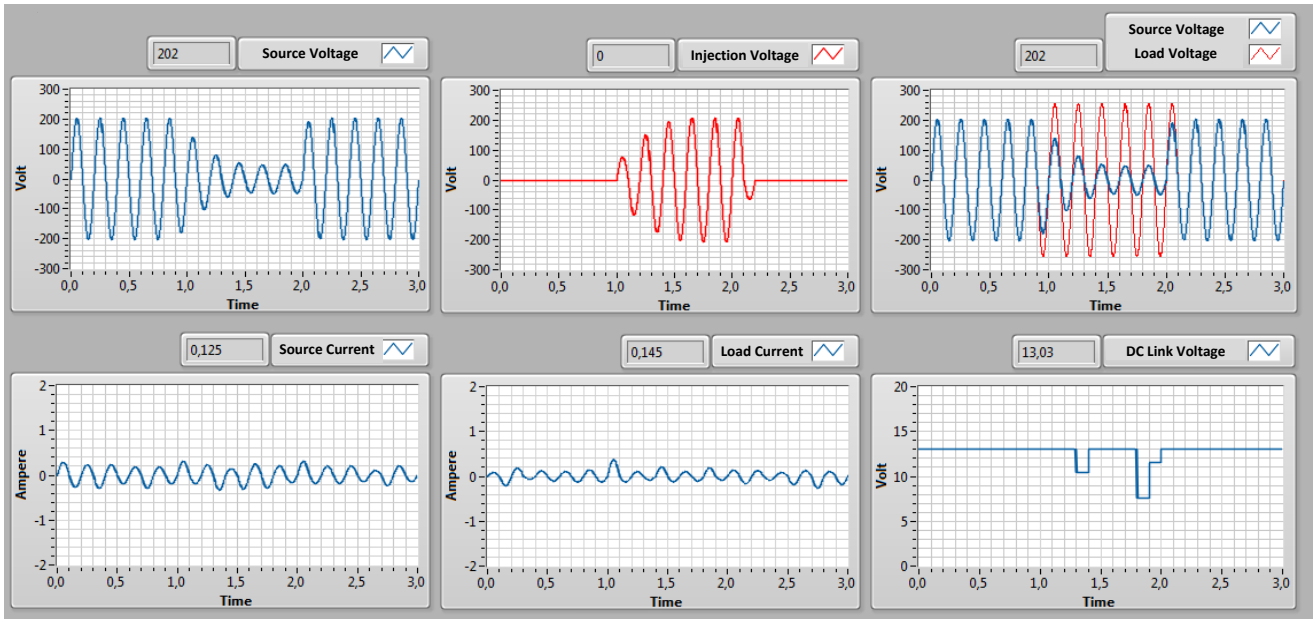

Figure. 7 Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to FL lamp load using LabVIEW

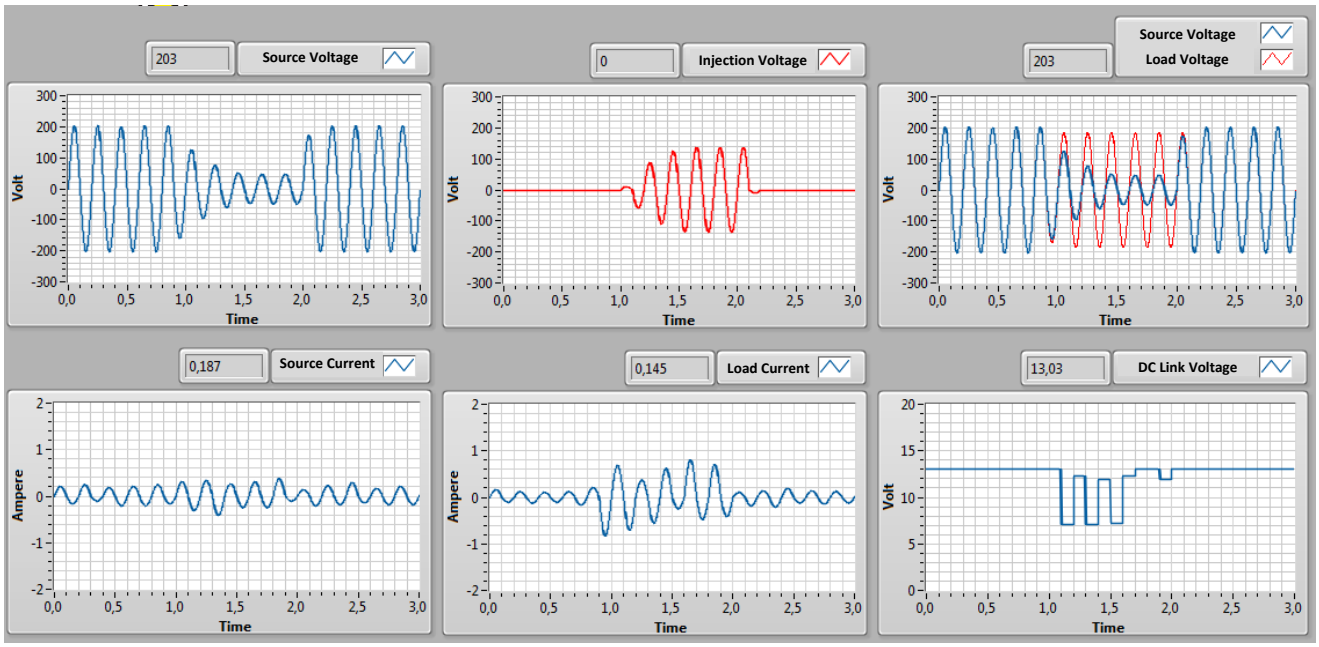

Figure. 8 Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to LED lamp load using LabVIEW

Fig. 6 shows the simulation curve of the sag voltage on a single-phase DVR system supplied by a BES connected to a bulb lamp load. The voltage sag disturbance lasts from t = 1 to t = 2 seconds with a total simulation time of 3 seconds. The measurements on all simulation parameters curves are carried out at t = 1.5 seconds. At t = 1 to t = 2 seconds, the source voltage (V_S) drops from 230 V to 44.7 V, and the series transformer injects a voltage (V_{Inj}) of 168 V so that the load voltage (V_L) remains constant at 216 V. In this disturbance condition the value of the source current (I_S) is 0.228 A and the load current (I_L) drops to 0.45 A. To keep the load voltage (V_L) maintain constant, BES releases its energy so that the DC link voltage ($V_{DC-Link}$) drops from 13.03 V to 8.20 V.

Fig. 7 shows the simulation curve of sag voltage on a single-phase DVR system supplied by the connected BES to the FL lamp load. At t = 1 to t = 2 seconds, the source voltage (V_S) drops from 230 V to 50.3 V and the series transformer injects a voltage (V_{Inj}) of 200 V so that the load voltage (V_L) remains

constant at 256 V. During the duration of the sag voltage, the capacitance effect of the capacitor component able to store charge on the FL lamp load, causing the load voltage value to exceed the source voltage. In the disturbance conditions, the value of the source current (I_S) is 0.166 A and the load current (I_L) drops to 0.208 A. To keep the load voltage (V_L) maintain constant, BES releases its energy so that the DC link voltage ($V_{DC-Link}$) drops from 13.03 V to 7.33 V.

Fig. 8 shows a simulation curve voltage sag on a single-phase DVR system supplied by BES connects to the LED lamp load. At t = 1 to t = 2 seconds, the source voltage (V_S) drops from 230 V to 49.1 V and the series transformer injects a voltage (V_{Inj}) of 133 V so that the load voltage (V_L) remains constant at 185 V. During the disturbance conditions, the value of the source current (I_S) is 0.249 A, and the load current (I_L) increases to 0.789 A. To keep the load voltage (V_L) maintain constant, BES then releases its energy so that the DC link voltage ($V_{DC-Link}$) drops from 13.03 V to 8.06 V.

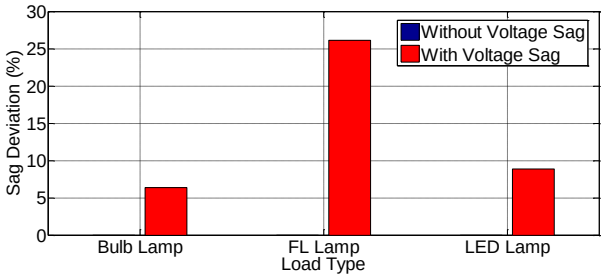

Figure. 9 Performance of sag deviation of V_L for single phase DVR-BES system on three load type

Fig. 9 shows that for the system without sag voltage, the series active filter circuit and series transformer on a single-phase DVR-BES system is not able to inject voltage into the load, so produces a percentage of sag deviation of load voltage (V_L)of 0%. Otherwise if the system with sag voltage, the single-phase DVR-BES system is able to maintain the load voltage (V_L) i.e. bulb lamp, FL lamp, and LED lamp of 216 V, 256 V, and 185 V, respectively. The percentage of load voltage deviation for the system with sag deviation of V_L for the three loads type are 6.4%, 26.13%, and 8.87%, respectively.

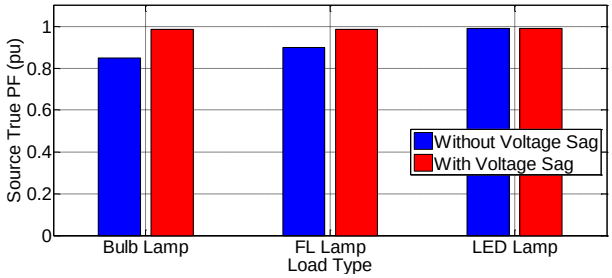

Figure.10 Performance of source true power-factor for single phase DVR-BES system on three load type

Fig. 10 shows the measurement of source true power-factor without voltage sag of the bulb lamp has the worst true power-factor (Pf_{true}) of 0.850 per-unit (pu) leading compared to an FL lamp of 0.900 pu leading and an LED lamp of 0.909 pu leading. Otherwise, for the system with voltage sag, the single-phase DVR-BES system produces source true power factor (Pf_{true}) for a bulb lamp, FL lamp, and LED lamp of 0.985 pu leading, 0.985 pu leading, and 0.990 pu leading respectively.

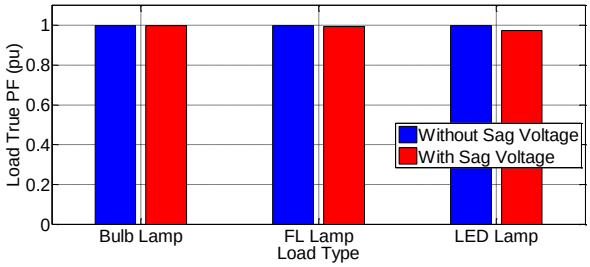

Figure. 11 Performance of load true power-factor for single phase DVR-BES system on three load type

Fig. 11 shows the measurement of load true power-factor without voltage sag for all load categories results in the same true power factor (Pf_{true}) of 0.999 pu leading. Otherwise, for the system with voltage sag is able to result in load true power factor (Pf_{true}) i.e. bulb lamp, FL lamp, and LED lamp of 0.975 pu leading, 0.998 pu leading, and 0.994 pu leading respectively.

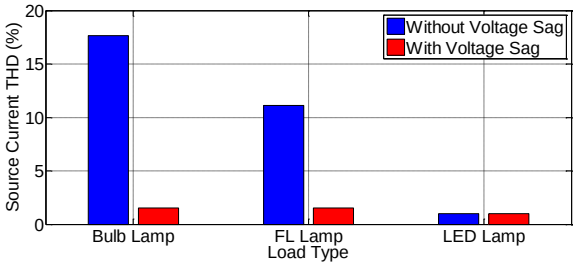

Figure. 12 Performance of source harmonics for single phase DVR-BES system on three load type

Fig. 12 shows that the system without sag voltage is able to produce the source THD_I for bulb lamp, FL lamp, and LED lamp of 17.647%, 11.111%, and 1.010% respectively. Otherwise, for the same system with sag voltage is able to result source THD_I. for bulb lamp, FL lamp, and LED lamp of 1.523%, 1.523%, and 1.010% respectively.

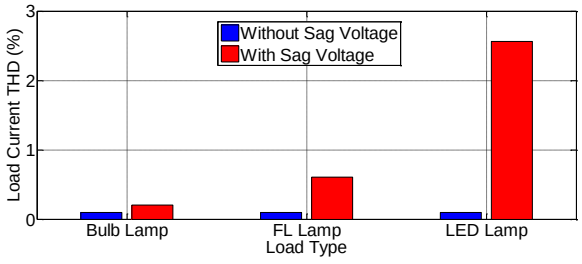

Figure. 13 Performance of load harmonics for single phase DVR-BES system on three load type

Fig. 13 shows that the system without voltage sag is able to produce the same load THD_I for bulb lamp, FL lamp, and LED lamp of 0.1001%. Otherwise, for the same system with voltage sag is able to result in load THD_I for bulb lamp, FL lamp, and LED lamp of 0.204%, 0.604%, and 2.564% respectively. Fig 10 and Fig. 11 shows in the case of voltage sag and three types of loads, the LHE lamp is able to result in the best performance because it is able to produce the highest source true power factor (Pf_{true}) of 0.990 pu and the lowest source THD_I of 1.010%. The source THD_I and load THD_I value in voltage sag also had met the IEEE 519.

Table 6. Comparison of implementation UVTG-DVR-BES-Arduino-Uno-LabVIEW (proposed study) and previous studies

No.	Authors	Methods	Depth Sag of V_S (%)	Sag Dev of V_L(%)	Load THD_V (%)	Source THD_I(%)	Source pf_{true}	Real Time
1	D.N. Katole, et.al [8]	Improved SRF	42	7.6	NA	NA	NA	Not
2	M.T. Hagh, et.al. [10]	FLC	92 without and 95 with DG	8.9 without DG and 6.4 with DG	1.26 without DG and 3.54 with DG	NA	NA	Not
3	H.K. Yada, et. al [16]	SOGI-PLL	30	3.0	NA	NA	NA	Not
4	S. Galeshi, et. al. [17]	Multilevel Cascade H-Bridge Inverter	20	0.0	4.0	NA	NA	Not
5	R. Nittala, et.al [19]	IDVR with VSI and CSI	27.7 with VSI and CSI	0 with VSI and CSI	0.06 with VSI and 0.05 with CSI	NA	NA	Not
6	E. Babaei, et. al. [22]	Direct Converter	65	0	7.07 (Average)	NA	NA	Not
7	A. Benhail, et.al. [23]	TDVR-PI	30	2.18	24	NA	NA	Not
8	J. Ye, et.al. [26]	Elliptical Restoration	60	NA	NA	NA	0.75	Not
9	R. Omar, et.al [28]	DVR-Super-capacitor	30	0	NA	2.38	NA	Not
10	C.K. Sundara-balan, et. al. [29]	CAESPDVR-ANFIS	46.67 (Average)	0.4	2.35	NA	NA	Not
11	V.K. Awaar, et.al. [31]	VSI-SPWM-NI-myRIO-1900-Labview	50	8.79	NA	NA	NA	Yes
12	A.Kiswantono et.al. [32]	UVTG-DVR-BES-PV	80	2.89 (Average)	5.81 (Average)	NA	NA	Not
13	**Proposed Study**	**UVTG-DVR-BES-Arduino-Uno-Labview**	**80**	**Bulb=6.4 FL =26.13 LED=8.87**	**NA**	**Bulb=1.523 FL=1.523 LED=1.010**	**Bulb=0.985 FL=0.985 LED=0.990**	**Yes**

Note: NA = note available

Table 6 shows the validation of the results for the proposed study compared to the 12 previous studies. The parameters observed are depth of sag of V_S, sag deviation of V_L, load THD_V, source THD_I, and real-time simulation. At [8], D.N. Katole, et.al proposed an improved SRF on the single-phase DVR series. With a depth of sag of V_S of 42%, this method produces a sag deviation of V_L of 7.6%. Furthermore, the FLC method for sag stress compensation was proposed by M.T. Hagh, et.al [10]. With a depth of sag of V_S of 92% without and 95% with DG, the FLC method yields a sag deviation of V_L of 8.9% without DG and 6.4% with DG, and a load THD_V of 1.26% without DG and 3.54 with DG. The SOGI-PLL

method proposed by Yada et. Al [16], with a depth of sag of V_S of 30% was able to produce a sag deviation of V_L of 3.0%. S. Galeshi, et. al [17] already offer Multilevel Cascade H-Bridge Inverter topology. With a depth of sag of V_S of 20%, this topology produces a sag deviation of V_L of 0% and a load of THD_V of 4%. IDVR configuration with VSI and CSI has been proposed by R. Nittala, et.al [19]. With a depth of sag of V_S of 27.7% (with VSI and CSI), this configuration resulted in a sag deviation of V_L of 0%, load THD_V of 0.06% (with VSI) and 0.05% (with CSI). E. Babaei, et. al [22] have proposed a direct converter topology to mitigate voltage sag. With a depth of sag of V_S of 65%, this topology produces a sag deviation of V_L of 0% and a load THD_V of 7.07% (average).

The TDVR-PI configuration has been proposed by A. Benhail, et.al. [23]. With a depth sag of V_S, of 30%, this configuration results in a sag deviation of V_L of 2.18% and a load THD_V of 24%. J. Ye, et.al [26] have proposed an elliptical restoration method for voltage sag compensation and power factor correction. With a depth of sag of V_S, of 60%, this method is able to produce a source pf_{true} of 0.75 pu. The DVR-Super-capacitor configuration has been implemented by R. Omar, et.al [28]. With a depth of sag of V_S, of 30%, this topology is able to produce a sag deviation of V_L of 0 % and source THD_I of 2.38%. The CAESPDVR-ANFIS topology has been investigated by C.K. Sundarabalan, et. al. [29]. With a depth of sag of V_S, of 46.67% (average), this topology was able to produce a sag deviation of V_L of 0.4% and a load of THD_V of 2.35%. V.K. Awaar, et.al. [31] have implemented a VSI-SPWM-based single-phase DVR model with the NI-myRIO-1900 interface monitored in real-time by LabVIEW. With a depth of sag of V_S, of 50%, this model was able to produce a sag deviation of V_L of 8.79%. DVR control supplied by BES-PV using the UVTG method has been observed by A. Kiswantono [32]. With a depth of sag of V_S, of 80%, this configuration and method were able to produce a sag deviation of V_L of 2.89% (average) and a load THD_V of 5.81% (average). Based on the results of research [31] and [32], then this study has implemented the single-phase DVR model using the UVTG method with the Arduino-Uno interface monitored in real-time by LabVIEW. With a depth of sag of V_S of 80%, the proposed model is able to produce sag deviation of V_L of 6.4% (Bulb), 26.13% (FL), and 8.87% (LED). The model is also able to produce THD_I source of 1.523% (Bulb), 1.523% (FL), and 1.101% (LED) and pf_{true} respectively 0.985% (Bulb), 0.985% (FL), and 0.909% (LED). The proposed study is able to give the best performance because it is able to produce source THD_I lower than [28] and source pf_{true} is higher than [26]. Another contribution is that by using the Arduino-Uno interface, the proposed model can be run and monitored in real-time with LabVIEW. It is different from the simulations conducted by 12 previous researchers (except [31]) which were still carried out off-line using Matlab/Simulink environment.

4. Conclusion

The system using a single-phase DVR supplied by BES with load voltage controlled by a UVTG method has been implemented. The model is connected to three types of linear/non-linear load i.e. bulb lamp, FL lamp, and LED lamp. This configuration is proposed to mitigate 80% voltage sag using the Arduino-Uno hardware and monitored by LabVIEW simulation in real-time. The investigated parameter are source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power-factor measurements are also carried out to obtain the harmonics of the source current and load current. During voltage sag, the single-phase DVR-BES system is able to maintain load voltage for all types of loads. From the system with voltage sag and three different types of loads, the LHE lamp is able to result in the best performance because it is able to produce the highest source current power factor (pf_{true}) and the lowest source THD_I. The source THD_I and load (THD_I) with voltage sag also had met the IEEE 519. The proposed study is able to give the best performance because it is able to produce source THD_I lower than the previous studies. By using the Arduino-Uno interface, this model can be run and monitored in real-time with LabVIEW better from the simulations conducted by previous researchers which were still carried out off-line using Matlab/Simulink.

In a system using a single-phase DVR-BES connected to the FL load, there is a significant increase in load voltage of 256 V compared to the source voltage. The percentage of sag voltage for FL lamps also increased by 26.13% and has far exceeded the value of 5%. The implementation of a single-phase bidirectional inverter circuit as the interface between the BES and series active filters can be proposed as future work to overcome this problem. The measurement of source THD_V and load THD_V in the proposed model is also necessary to determine the harmonic mitigation performance of the voltage within the IEEE 519 limit.

Conflicts of Interest

The authors declare no conflict of interest.

Author Contributions

Conceptualization, Y.A. Setiawan and A. Amirullah; methodology, Y.A. Setiawan and A. Amirullah; software, Y.A. Setiawan; validation, Y.A. Setiawan; formal analysis, Y.A. Setiawan and A. Amirullah; investigation, Y.A. Setiawan and A. Amirullah; resources, Y.A. Setiawan; data curation, Y.A. Setiawan; writing—original draft preparation, Y.A. Setiawan; writing—review and editing, Y.A. Setiawan; visualization, Y.A. Setiawan; supervision, A. Amirullah; project administration, Y.A. Setiawan; funding acquisition, A.Amirullah. All authors read and approved the final manuscript.

Acknowledgements

The authors would like to acknowledge to Institutions of Research and Community Service Universitas Bhayangkara Surabaya, for funding to this research base on Decree Letter Number 65/XI/2020/UBHARA date 19 November 2020.

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Paper ID	**3819**
Paper Title	**Implementation of Single-Phase DVR-BES Based on Unit Vector Template Generation (UVTG) to Mitigate Voltage Sag Using Arduino Uno and Monitored in Real-Time Through LabVIEW Simulation**
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Implementation of Single-Phase DVR-BES Based on Unit Vector Template Generation (UVTG) to Mitigate Voltage Sag Using Arduino Uno and Monitored in Real-Time Through LabVIEW Simulation

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Abstract: This paper aims to design and implement a single-phase dynamic voltage restorer (DVR) supplied by battery energy storage (BES) using load voltage controlled by the unit vector template generation (UVTG) method. The UVTG method on the DVR system is implemented using the Arduino-Uno hardware. LabVIEW-based interface simulation is used for monitoring the parameter in real-time during 80% voltage sag period i.e. source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power factor measurements are also carried out to obtain total harmonic distortion (THD) of the source current and load current. The single-phase DVR system is connected to load i.e. a 5-watt bulb lamp (linear-load), 5-watt fluorescent (FL) lamp (non-linear load), and 5-watt light-emitting diode (LED) lamp (non-linear load). During voltage sag, the single-phase DVR-BES system is able to maintain load voltage i.e. bulb lamp, FL lamp, and LED lamp of 216 volts, 256 volts, and 185 volts, respectively. The percentage of load sag voltage deviation for each load is 6.4%, 26.13%, and 8.87%, respectively. The measurement of source power-factor with voltage sag results in source true power factor of three loads of 0.985 pu leading, 0.985 pu leading, and 0.990 pu leading respectively. On the same system with voltage sag, single phase DVR-BES is able to result in source current THD for three loads of 1.523%, 1.523%, and 1.010% respectively. The proposed study is able to give the best performance because it is able to produce source current THD lower than the previous studies. By using the Arduino-Uno interface, this model can be run and monitored in real-time with LabVIEW better from the simulations conducted by previous researchers which were still carried out off-line using Matlab/Simulink.

Keywords: Single Phase DVR, BES, Arduino Uno, LabVIEW, Voltage Sag

1. Introduction

During the last decade, there has been an increase in the number of sensitive and critical loads. On the other hand, the use of these tools also has an impact on deteriorating Power Quality (PQ). Among a number of PQ problems, problems related to voltage mitigation are also of increasing importance from a sensitive load and customer point of view. PQ problems related to voltage i.e. voltage sag, voltage swell, voltage harmonics, fluctuations, interruptions, and imbalance. In accordance with IEEE 1346 [1] and IEEE 1159 [2] standards, the sag voltage is defined as the RMS (root mean square) AC voltage sag with a magnitude of 10% to 90% of the nominal voltage, at power frequencies with a duration of 0.5 cycles to one minute. The voltage sag is caused by a single-phase short circuit to ground in the power system, starting in large-capacity induction motors, and sudden changes in the system connected to large loads [3]. Viewed from the system, the DVR is divided into two systems, namely one-phase DVR and three-phase DVR. Then three-phase DVR is connected to a 3 phase 3 wire (3P3W) or a 3 phase 4 wire (3P4W) system. Next, this paper will further focus on the design and implementation of single-phase DVRs to mitigate voltage sag at the source side and connect to a number of the linear/non-linear load. The simulation of low voltage single phase DVR based on the multilevel inverter to protect sensitive loads has been implemented

in [4]. The proposed model is able to compensate for the voltage sag and increase the PQ on the load side. A DVR topology using a cascaded multilevel direct pulse with modulation (PWM) ac-ac converter has been proposed in [5]. In this scheme, the unit cell of the multilevel converter consists of a single-phase ac-ac converter PWM using a switching cell (SC) structure that is paired with an inductor. The implementation of the phase shift PWM technique is capable of significantly reducing the size of the output filter inductor. One and three-phase DVR control schemes using PSCAD/EMTDC have been observed in [6]. The proposed system is able to compensate for a number of voltage sag variations and keep the load voltage constant. DVR control scheme with an ac-ac converter, based on voltage drop characterization has been investigated in [7] to reduce voltage drop with phase jumps. The superiority of the proposed control scheme is then validated on an ac-ac interphase converter topology. The vector-based one-phase DVR control using an improved synchronous reference frame (SRF) has been proposed in [8]. The vector analysis used in this control method during the voltage period was able to provide the magnitude and phase of the injection voltage.

The control methods to reduce sag voltages using a fuzzy logic controller (FLC) connected with sensitive loads [9] and distributed generation (DG) [10] have been proposed. The FLC control was used to generate pulses with the Sinusoidal Pulse Width Modulation (SPWM) technique at the output of an active filter circuit. Comparing to proportional-integral (PI) control, FLC control was able to provide better performance during voltage sag because it has more advantages in terms of resistance to parameter variations and system execution. A DVR with DG-connected FLC control also able to enhance voltage profiles, power quality, and reliability. Single-phase and three-phase DVRs use a single-phase ac to ac matrix converter to replace voltage source inverter (VSI), has been investigated by Matlab in [11],[12], and in PSCAD [13], at a number of variations in source voltage (sag, flicker, and unbalance). The single-phase DVR has been simulated in [14] and a special voltage detection method for single-phase DVRs has been introduced in [15]. The simulation results show that the DVR was able to maintain the nominal load voltage, despite interference and other abnormal conditions from the source side. The special detection method using double closed-loops of the proportional-resonant controller was also able to provide superior performance in voltage detection and compensation.

The DVR control scheme for reference voltage generation based on a single-phase Second Order Generalized Integrator-Phase Lock Loop (SOGI-PLL) using a series of active compensator has been observed in [16]. The proposed scheme is capable of dynamically responding, detecting, and rapidly compensating for sag/swell voltages without and with phase jumps. A DVR that uses a multilevel H-bridge inverter with a capacitor as an energy source has been introduced in [17]. This configuration allows the DVR to connect directly to a medium-voltage network, eliminating the need for a series injection transformer and batteries. The DVR model was the same but uses a single H-Bridge inverter and a battery on sag/swell voltage disturbances connected to the non-linear load which has also been observed in [18]. Interline DVR (IDVR) on two same [19] and different voltage distribution lines with voltage source inverter (VSI) and current source inverter (CSI) [20] to restore voltage sag and harmonics has been introduced. When voltage sag and voltage distortion occur on one channel, the DVR on the same channel is able to perform voltage compensation and harmonics elimination, while the other DVR can recharge the energy to the DC-link to maintain the DC-link voltage constant.

In order to efficiently the number of equipment in the DVR circuit configuration, the implementation of a direct ac/ac converter on the DVR has been introduced in [21],[22]. The proposed configuration uses the minimum switches, did not require a dc-link energy storage element, and has a longer compensation time during sag/swell voltage disturbances. The compensation voltage for each phase is taken from each of the three-phase sources so that each converter was able to operate independently and is also able to compensate for single-phase blackouts and unbalance sag/swell voltages. The use of a single-phase transformer-less DVR (TDVR) to mitigate the sag/swell voltage has been observed in [23]. The proposed configuration was capable of reducing system size and losses compared to DVR which using a series transformer. The single-phase interactive channel DVR using the sag voltage detection algorithm has been developed in [24]. The detection algorithm has a hybrid structure consisting of a momentary detection section and a RMS variation detection section. The DVR development could compensate for input voltage sag or interrupt in 2.0-ms delay and can be used effectively for sensitive loads.

The single-phase DVR with synchronous reference frame control under distorted source conditions has been applied in [25]. The proposed control using a moving average filter (MAF) is capable of extracting positive sequence fundamental components as well as being able to mitigate voltages sag and distorted source voltages. The single-phase DVR using elliptical restoration-based voltage compensation to correct the power factor on the source side has been proposed in [26]. The active and reactive voltage components and centrifugal angles are

used to formulate an elliptical compensation path. So that the voltage will be in-phase with the load current using precise control of the DVR injection voltage. The optimization of the voltage injection technique in DVR to protect sensitive loads has been observed in [27]. The recursive least square (RLS) method is used to estimate the magnitude and phase of the voltage in order to minimize the amplitude of the injection voltage. Meanwhile, repetitive control was proposed to track the compensation voltage. Both controls are suitable for sinusoidal reference and are reliable for mitigating harmonics, sags, and swell distortions.

Energy storage in single or three-phase DVR circuits related to the capacity and type of energy storage has become the attention of many researchers. The determination of the two parameters relates to the ability and duration of the energy storage to supply real power to the inverter during a fault. Unbalanced voltage compensation in 3P3W system using DVR using a super capacitor has been investigated in [28]. The proposed DVR configuration uses a control based on the d-q-0 and Proportional Integral (PI) transformation technique and is further coded using a digital signal processor (DSP). DSP control and super capacitor implementation can mitigate unbalanced voltage disturbances. A compressed air energy storage powered dynamic voltage restorer (CAESPDVR) with ANFIS control has been proposed in [29] to compensate for unbalanced sag/swell voltages and harmonics. The single-phase DVR configuration using a hybrid energy storage system (HES) has been developed in [30].

The HES series consists of superconducting magnetic energy storage (SMES) in collaboration with battery energy storage (BES) on a DC type DVR. The proposed HES concept integrated with fast response large power SMES unit and low-cost high capacity BES can further be implemented in large scale DVR development. The DVR uses VSI method with SPWM to compensate for sag voltage has been implemented in [31]. The voltage sag was able to be simulated and monitored by LabVIEW with the NI myRIO-1900 interface using LabVIEW in real-time. The mitigation of sag/swell voltage and harmonics in low voltage distribution networks using DVR-BES-PV using the UVTG control method has been observed in [32]. The proposed model was able to compensate for sag voltage between 10% to 90% and swell voltage between 110% to 180% with a voltage THD within the IEEE 519 limit.

In this paper, BES is proposed as energy storage and implemented in single-phase DVR using load voltage control with the UVTG method and connected to linear/non-linear loads. The UVTG method on the DVR system is implemented using the Arduino-Uno microcontroller hardware. The LabVIEW based interface simulation is used to monitor electrical quantities in real-time during the voltage sag period i.e. source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power factor measurements are also carried out to obtain the total harmonic value or Total Harmonic Distortion (THD) of the source current and load current.

This paper is arranged as follows. Section 2 presents the proposed method, UVTG method, percentage of voltage sag, true power factor and harmonic, single-phase DVR-BES using LabVIEW, as well as hardware and software implementation, Section 3 presents results and discussion of the source voltage, injection voltage, load voltage, DC-link voltage, source current, load current, percentage of voltage sag, true power-factor, and current THD which analyzed from data measured by Arduino-Uno and monitored by LabVIEW. In this section, the system connected to the linear/non-linear load with and without voltage sag is selected to present the best performance single-phase DVR-BES system connected to three different types of load during voltage sag. Finally, this paper is concluded in Section 4.All manuscripts must be in English. These guidelines include complete descriptions of the fonts, spacing, and related information for producing your proceedings manuscripts. Table 1 shows the abbreviations used in this paper.

Table 1. Abbreviation

Symbol	Description
PQ	Power Quality
DVR	Dynamic Voltage Restorer
BES	Battery Energy Storage
PV	Photovoltaic
UVTG	Unit Vector Template Generation
THD	Total Harmonic Distortion
Pf_{true}	True Power Factor
FL	Fluorescent
LED	Light Emitting Diode
DG	Distributed Generation
3P3W	Three Phase Three Wire
3P4W	Three Phase Four Wire
SPWM	Sinusoidal Pulse Width Modulation
VSI	Voltage Source Inverter
CSI	Current Source Inverter
SOGI-PLL	Second Order Generalized Integrator-Phase Lock Loop
CAESPDVR	Compressed Air Energy Storage Powered Dynamic Voltage Restorer
ANFIS	Artificial Intelligent Fuzzy Inference System
IDVR	Interline Dynamic Voltage Restorer
CB	Circuit Breaker
RMS	Root Mean Square
GUI	Graphic User Interface
PC	Personal Computer
USB	Universal Serial Bus
PU	Per Unit

2. Research Method

2.1. Proposed Method

Fig. 1 shows a single-phase DVR supplied by BES using load voltage control with the UVTG method. The DVR is a tool that functions to compensate for the load voltage in the event of a voltage sag disturbance on the source bus at a level of 0.1 to 0.9 per unit. The UVTG method on the DVR system is implemented using the Arduino-Uno hardware. LabVIEW-based interface simulation is used to monitor electrical quantities in real-time during the voltage sag period.

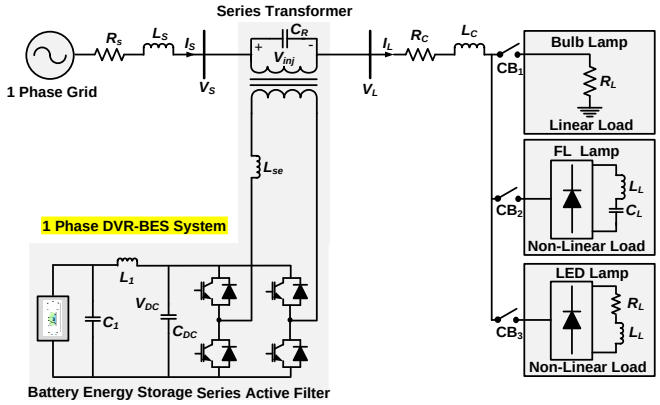

Figure. 1 Proposed single phase DVR-BES connected to linear/non-linear load

The observed parameters are source voltage (V_S), injection voltage (V_{inj}), load voltage (V_L), DC-link voltage ($V_{DC-Link}$), source current (I_S), and load current (I_L). The true power-factor (Pf_{true}) measurements are also carried out to obtain the THD value of the source current and load current. There are two cases in this study, the source without voltage sag, and with an 80% voltage sag. In each case, the single-phase DVR system is supplied by BES connected to a 5-watt bulb lamp (linear load), 5 watt FL lamp (non-linear load), and 5 watts LED lamp (non-linear load), so the total selected case is six. The CB1, CB2, and CB3 are used to connect and disconnect links to three linear/non-linear loads. The DVR-BES system configuration is then run based on a predetermined case using Arduino-Uno microcontroller interfaced communication and the results are simulated and monitored in real-time by a LabVIEW. Table 2 shows the notation list and parameters of Fig. 1.

Table 2. Notation list and parameters

Notation	Description
V_S	Source Voltage
V_{inj}	Injection Voltage
V_L	Load Voltage
$V_{DC-Link}$	DC-Link Voltage
I_S	Source Current
I_L	Load Current
I_L^*	Reference Load Voltage
V_m	Peak Fundamental Input Voltage Magnitude
K	Gain
S_1, S_2, S_3, S_4	Gating Signal 1, 2, 3, and 4
Sag_{dev}	Voltage Sag Deviation
$V_{pre-sag}$	Pre-Sag Voltage
V_{sag}	Sag Voltage
Pf_{true}	True Power Factor
P_{avg}	Average Power
S	Apparent Power
V_{rms}	RMS Voltage
I_{rms}	RMS Current
V_{1rms}	RMS Fundamental Voltage
I_{1rms}	RMS Fundamental Current
THD_V	Voltage THD
THD_I	Current THD
P_{1avg}	Fundamental Average Power
$Pf_{displacement}$	Displacement Power Factor
$Pf_{distorted}$	Distorted Power Factor
R_S	Line Resistance (0.1 ohm)
L_S	Line Inductance (0.15 mH)
R_C	Load Resistance (0.4 ohm)
L_C	Load Inductance (15 mH)
L_{Se}	Series Inductance (0.015 mH)
L_1	BES Inductance (6 mH)
C_1	BES Capacitance (1000 µF)
C_{DC}	DC-Link Capacitance (200 µF)
R_L	Linier/Non-Linear Resistance (0.6 ohm)
L_L	Non-Linear Load Inductance (0.15 mH)
C_L	Non-Linear Load Capacitance (3.3 µF)
C_R	Ripple Capacitance (0.2 µF)

2.2. Unit Voltage Template Generation Method

The series active filter protect sensitive loads against several voltage disturbances from the source bus. In [31], the control method of source and load voltage in a three-phase series active filter has been discussed. Using the same procedure, the authors propose the same method for single-phase series active filter control as shown in Fig. 2. This method extracts UVTG from the distorted input supply. Then, the template is expected to be an ideal sinusoidal signal with a unity amplitude. The source of the distorted voltage is measured and divided by the peak amplitude fundamental input voltage (V_m).

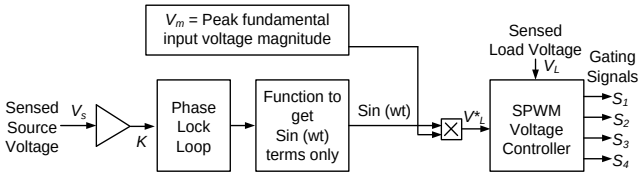

Figure. 2 UVTG control on single phase series active filter

A single-phase locked loop (PLL) is used in order to generate sinusoidal unit vector templates with a phase lagging by the use of the sine equation. The

reference signal of the load voltage is calculated by multiplying the unit vector templates with the peak amplitude of the fundamental input voltage (V_m). The reference load voltage (V_L^*) is then compared to the sensed load voltage (V_L) by a SPWM controller used to generate the desired four gating signal on a single-phase series active filter.

2.3. Percentage of Voltage Sag Deviation

The recommended standard of practice on monitoring voltage sag/swell as part of electric power quality parameters is IEEE 1159 [2]. This standard presents the definition and table of voltage sag base on categories (instantaneous, momentary, temporary) typical duration, and typical magnitude. The percentage of load voltage sag deviation is formulated in Eq. (1) [31].

$$Sag_{dev}(\%) = \frac{|Vpre\_sag - V\_sag|}{Vpre\_sag} \quad (1)$$

2.4. True Power Factor and Harmonics

The true power factor at the load is defined as the ratio of average power to apparent power. The true power factor for both sinusoidal and non-sinusoidal situations is presented in Eq. (2) [33].

$$pf_{true} = \frac{P_{avg}}{S} = \frac{P_{avg}}{V_{rms}\, I_{rms}} \quad (2)$$

$$V_{rms} = V_{1rms}\sqrt{1 + (THD_V/100)^2} \quad (3)$$

$$I_{rms} = I_{1rms}\sqrt{1 + (THD_I/100)^2} \quad (4)$$

By substituting Eq. (3) and Eq. (4) into Eq. (2), the true power factor (Pf_{true}) results in Eq. (5) for both sinusoidal and non-sinusoidal cases [33].

$$pf_{true} = \frac{P_{avg}}{V_{1rms}\, I_{1rms}\sqrt{1+(THD_V/100)^2}\sqrt{1+(THD_I/100)^2}} \quad (5)$$

A useful simplification can be made by expressing Eq. (5) as a product of two components defined in Eq. (6).

$$pf_{true} = \frac{P_{avg}}{V_{1rms}\, I_{1rms}} \times \ldots\ldots \frac{1}{\sqrt{1+(THD_V/100)^2}\sqrt{1+(THD_I/100)^2}} \quad (6)$$

By making the following two assumptions: (1) In most cases, the contributions of harmonics above the fundamental to average power are very small, so that is $P_{avg} \approx P_{1avg}$ and (2) Since THD_V is less than 10%, then from (12) we see that $V_{rms} \approx V_{1rms}$. Then, merging both assumptions into Eq. (6) results in the following approximate function for the true power factor (Pf_{true}) presented in Eq. (7) [33].

$$pf_{true} = \frac{P_{1avg}}{V_{1rms}\, I_{1rms}} \times \frac{1}{\sqrt{1+(THD_I/100)^2}} = Pf_{displacement} \times Pf_{distorted} \quad (7)$$

Because displacement power factor (Pf_{disp}) could never be greater than unity, Eq. (7) shows that the true power factor (Pf_{true}) in non-sinusoidal cases has the upper limit so finally its function is defined in Eq. (8) [33].

$$pf_{true} \le Pf_{distorted} = \frac{1}{\sqrt{1+(THD_I/100)^2}} \quad (8)$$

2.5. Single Phase DVR-BES using LabVIEW

The implementation of the single-phase DVR-BES system consists of several stages. That stage i.e. create a single-phase series active filter, create a gate driver to trigger the MOSFET in the series active filter, create a SPWM program to drive the gate driver as an inverter trigger and create a monitoring program in LabVIEW. Fig. 3 presents a schematic diagram of a single phase DVR-BES system.

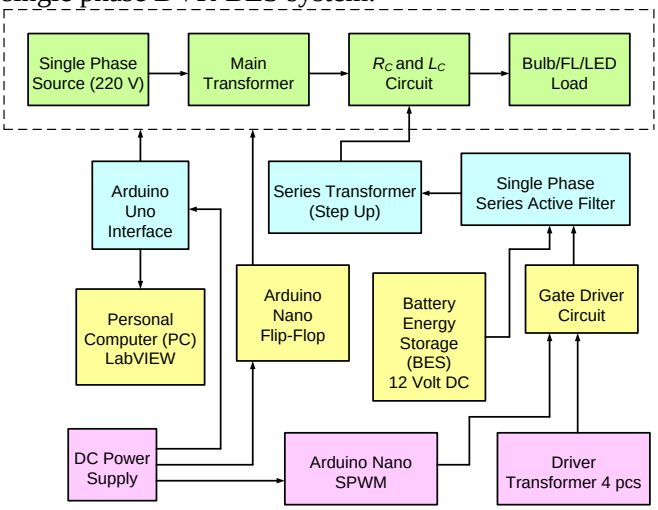

Figure. 3 A schematic diagram of single phase DVR-BES

Fig. 3 shows that the BES and series active filters play an important role in compensating for the voltage sag on a single-phase DVR. The step-up transformer that is installed in a series against the load functions to inject the voltage from the series active filter to the load. The main energy source for series active filters uses BES DC voltage 12 V with a capacity of 7.2 Ah. The process of changing the DC to AC voltage begins with the Arduino Nano SPWM microcontroller providing Sinusoidal SPWM pulses to the Gate Driver circuit which has the main component of the TLP 250 Optocoupler IC, then the Gate Driver circuit triggers the IRFP250 MOSFET gate on a series active filter circuit cross-like as an electric current cycle in the circuit bridge diode rectifier. So that it will produce an AC output from a series active filter circuit. The output voltage of the series active filter is an AC

voltage of 7 V depending on the battery voltage conditions, which will then be increased to an AC voltage of 220 V using a step-up transformer. The step-up series transformer has a power of 600 VA with a primary AC input voltage of 7.2 V and a secondary AC output voltage of 220 V. The goal is that the series active filter is able to inject enough power to compensate for the sag voltage at a level of 10% to 90%.

The Arduino Nano flip-flop functions as a timer to run system simulations using a single-phase DVR-BES without and with sag voltage. The Arduino nano has been programmed with a flip-flop program with the 1-second case instructing the relay to turn "on" as a representation of the system experiencing sag voltage and 1 second ordering the relay to turn "off" as a representation of the system without experiencing sag voltage. This timer is expected to function when there is a sag voltage and automatically orders a single-phase active filter to inject a voltage compensation into the load so that the load voltage will remain stable.

The Arduino Uno interface functions as a medium for receiving data from voltage sensors and current sensors that are measuring the amount of electricity in the DVR circuit and sending the data to a personal computer (PC) with LabVIEW software. Curves and data displayed in LabVIEW i.e. source voltage, load voltage, injection voltage, DC-link voltage, source current, and load current respectively. The display form implemented in LabVIEW is in the form of graphs and number indicators. With a graphic display, the reader will find it easier to observe the wave condition both voltage and current during the system condition without and with voltage sag. All data displayed in LabVIEW is real-time and continuous data as long as the single-phase DVR-BES system is operated to the system. In addition to using the LabVIEW, data collection is also carried out by the cos-phi meter to determine the value of the true power factor of source and load as a basis for determining the harmonic of source and load currents. The single-phase DVR-BES system connected to three linear/non-linear loads i.e. bulb lamp 5 W (linear), FL lamp 5 W (non-linear), LED lamp 5 W (non-linear) respectively.

2.6. Hardware and Software Implementation

The LabVIEW interface software diagram consists of the main program in the form of a Graphic User Interface (GUI) which functions to run all indicators and controls on the front panel. Fig. 4 shows the model of the single-phase DVR-BES hardware circuit. The nominal parameters of Fig. 4 are presented in Table 3.

Table 3. Nominal of device parameters

Devices	Design Values
Single phase source voltage	220 V
Frequency	50 Hz
Series Transformer (*step-up)*	600 VA 7,2/220 V
Main Transformer (CT)	3 A
Current Sensor ACS 712	5A
Relay	1 device
Arduino Uno (Interface)	1 device
Arduino Nano (Flip-Flop)	1 device
Arduino Nano (SPWM))	1 device
Load Resistance (R_C)	0.4 ohm
Load Inductance (L_C)	15 mH
Cos-phi-Meter	1 device
Battery Energy Storage (BES)	12 V/7.2 Ah
DC-link Capacitance (C_{DC})	1000 μF
Bulb Lamp Load	5 W
FL Lamp Load	5 W
LED Lamp Load	5 W

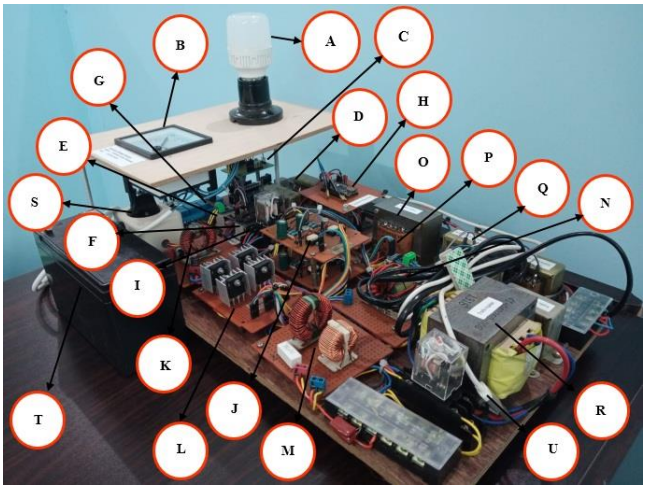

Figure. 4 Single-phase DVR-BES hardware

Where A: Load; B: Cos-phi-meter; C: Arduino Uno; D: Voltage Sensor Transformer; E: Current Sensor; F: Arduino Nano SPWM; G: Relay 1 (4 Channel); H: Arduino Nano Flip-Flop; I: Two Relays (220V-AC); J: Gate Driver Optocoupler; K: DC-link Capacitance and BES filter (C_{DC}, L_1, C_1); L: Series Active Filter; M: Load Impedance (R_C, L_C); N: Series Inductance (L_{Se}); O: Main Transformer; P: Source Current Sensor; Q: Gate Driver Transformer; R: Series Transformer; S: Source Voltage; T: BES and U: Universal Serial Bus (USB) for data communication between hardware PC.

Fig. 5 shows the overall GUI program design and the component parts of the single-phase DVR-BES. In order for the LabVIEW software interface on the PC to communicate with the Arduino Uno, a program is needed to communicate the two devices. The communication program used by Lifa Base. Lifa Base is the driver for Arduino Uno in connecting data communication with PC. Lifa Base is the default program from Arduino when users install LabVIEW.

3. Results and Discussion

Fig. 1 shows a series of DVR supplied by BES connected to a load of Bulb, FL, and LED respectively. The series transformer connected to the load functions to inject the voltage from the series active filter during voltage sag. The Arduino Nano Flip-Flop is used as a timer to run simulated data collection. The cycle timer applied to the DVR is 1 second on and 1 second off. The data collection period is carried out with a LabVIEW simulation for 3 seconds, with 80% depth of source voltage sag duration between 1 to 2 seconds. Data collection is carried out at 1.5 seconds from the curve of the source voltage (V_S), injection voltage (V_{inj}), load voltage (V_L), DC-link voltage ($V_{DC-Link}$), source current (I_S), and load current (I_L), curves. The true power-factor (Pf_{true}) data in the source bus and load bus is measured from the cos-phi meter.

Using the same LabVIEW simulation procedure and period, data collection is also carried out without the voltage sag. The percentage of load voltage sag deviation is calculated using Eq. (1) with a pre-sag voltage of 203 V. Base on true power-factor, then harmonics current is measured using Eq. (8). Table 4 presents the performance of voltage, current, and percentage of sag deviation of load voltage (V_L) of the single-phase DVR supplied by BES without and with voltage sag disturbance. Table 5 presents the performance of true power factor (Pf_{true}) and harmonics value of the single-phase DVR supplied by BES without and with voltage sag disturbance. Fig. 6, Fig. 7, and Fig. 8 show the performance of voltage and current of the single-phase DVR supplied by BES connecting to bulb lamp, FL lamp, and LED lamp load respectively.

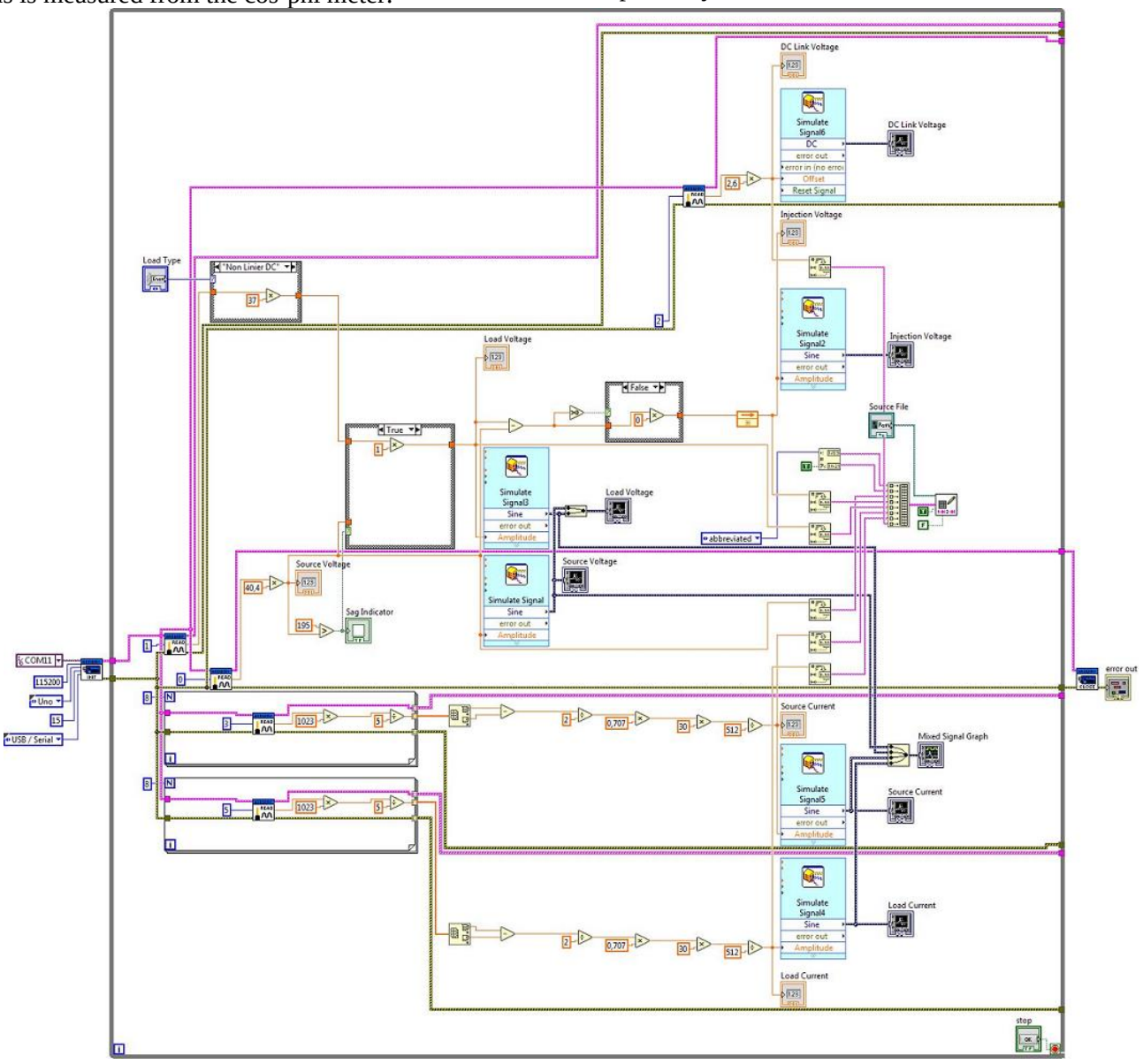

Figure. 5 Software design using LabVIEW interface for simulate signal i.e. (A) arduino-uno data communication, (B) source voltage (V_S), (C) injected voltage (V_{Inj}), (D) load voltage (V_L), (E) source current (I_S), (F) load current (I_L), (G) DC-link voltage ($V_{DC-Link}$), and (H) mixed signal graph

Table 4. Performance of voltage, current, and sag deviation of load voltage of the single-phase DVR supplied by BES

No.	Load Type	V_S (V)	$V_{Inj}(V)$	V_L (V)	I_S (A)	I_L (A)	$V_{DC-Link}$ (V)	Sag Dev of V_L (%)
Without Voltage Sag								
1.	Bulb Lamp	203	0	203	0.208	0.166	13.03	0
2.	FL Lamp	203	0	203	0.208	0.083	13.03	0
3.	LED Lamp	203	0	203	0.270	0.166	13.03	0
With Sag Voltage								
4.	Bulb Lamp	44.7	168	216	0.228	0.145	8.20	6.40
5.	FL Lamp	50.3	200	256	0.166	0.208	7.33	26.13
6.	LED Lamp	49.1	133	185	0.249	0.789	8.06	8.87

Table 5. Performance of power factor and harmonics of the single-phase DVR supplied by BES

No.	Load Type	Source Pf_{true} (pu)	Load Pf_{true} (pu)	Source THD_I (%)	Load THD_I (%)
Without Voltage Sag					
1.	Bulb Lamp	0.850	0.999	17.647	0.1001
2.	FL Lamp	0.900	0.999	11.111	0.1001
3.	LED Lamp	0.990	0.999	1.010	0.1001
With Sag Voltage					
4.	Bulb Lamp	0.985	0.998	1.523	0.2040
5.	FL Lamp	0.985	0.998	1.523	0.6040
6.	LED Lamp	0.990	0.975	1.010	2.5640

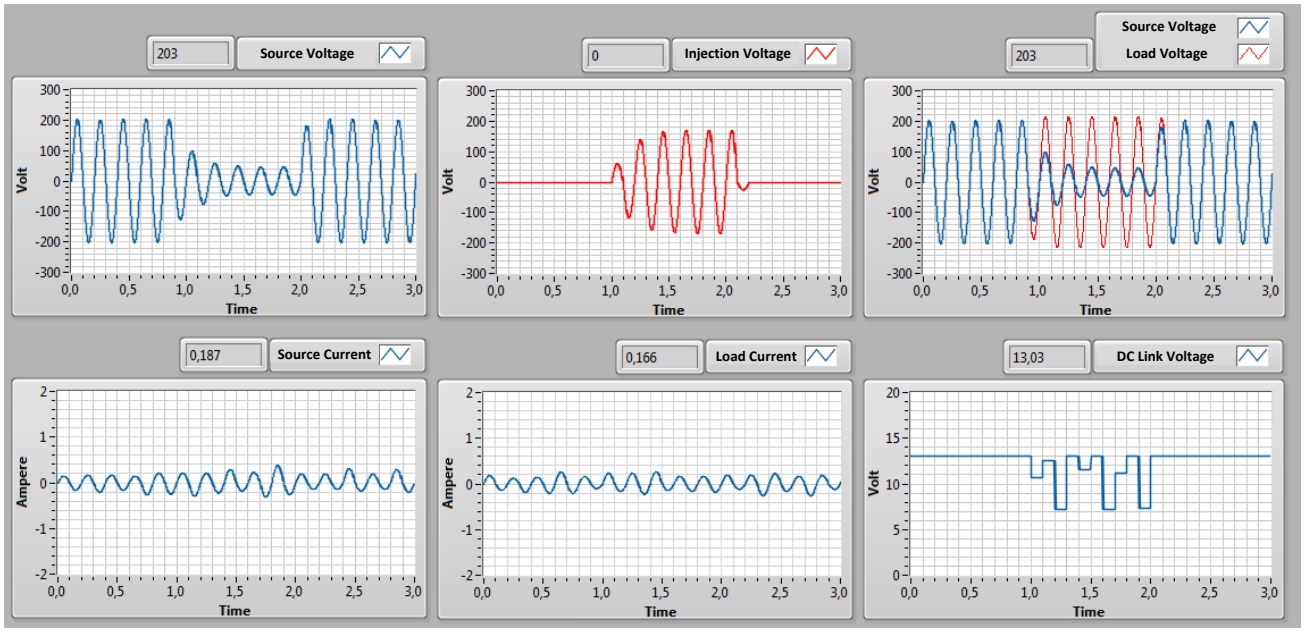

Figure. 6 Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to bulb lamp load using LabVIEW

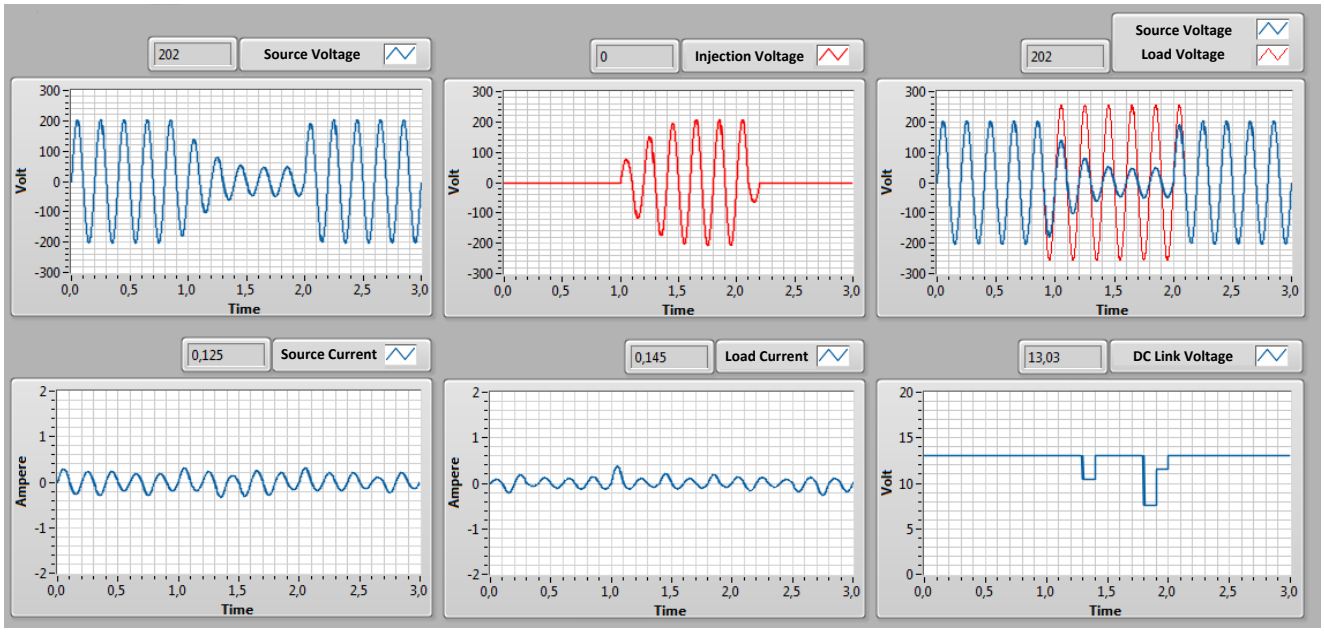

Figure. 7 Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to FL lamp load using LabVIEW

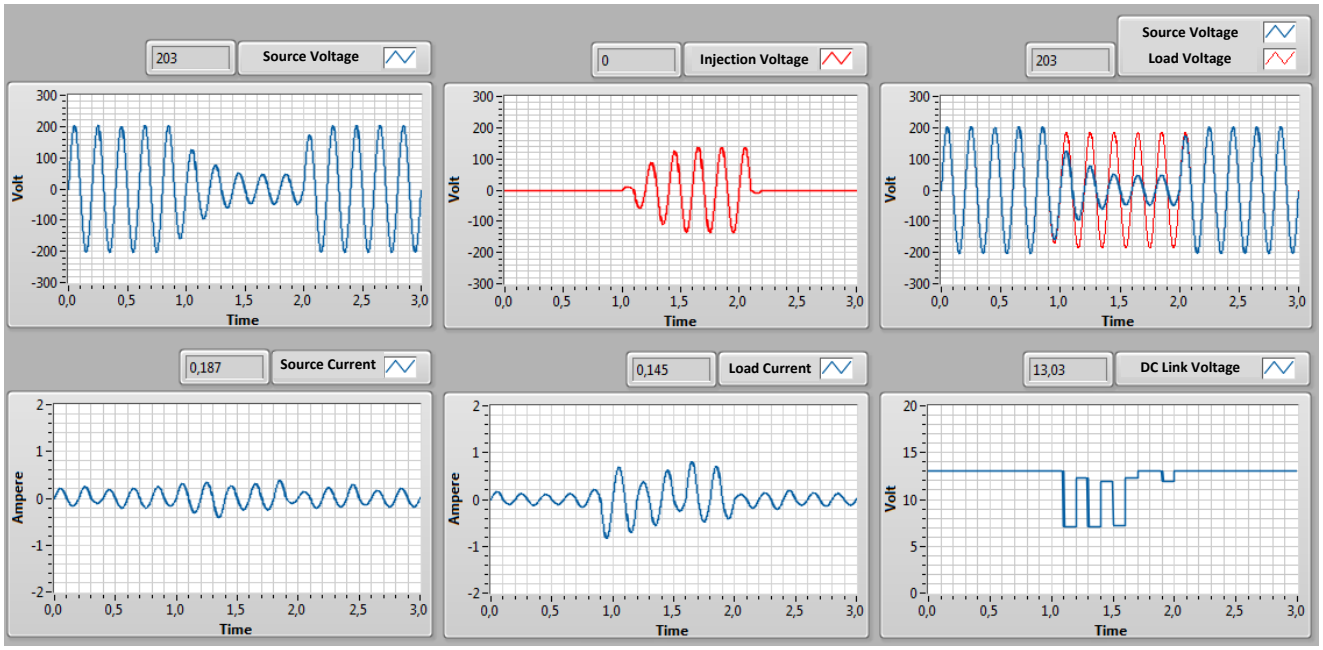

Figure. 8 Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to LED lamp load using LabVIEW

Fig. 6 shows the simulation curve of the sag voltage on a single-phase DVR system supplied by a BES connected to a bulb lamp load. The voltage sag disturbance lasts from t = 1 to t = 2 seconds with a total simulation time of 3 seconds. The measurements on all simulation parameters curves are carried out at t = 1.5 seconds. At t = 1 to t = 2 seconds, the source voltage (V_S) drops from 230 V to 44.7 V, and the series transformer injects a voltage (V_{Inj}) of 168 V so that the load voltage (V_L) remains constant at 216 V. In this disturbance condition the value of the source current (I_S) is 0.228 A and the load current (I_L) drops to 0.45 A. To keep the load voltage (V_L) maintain constant, BES releases its energy so that the DC link voltage ($V_{DC-Link}$) drops from 13.03 V to 8.20 V.

Fig. 7 shows the simulation curve of sag voltage on a single-phase DVR system supplied by the connected BES to the FL lamp load. At t = 1 to t = 2 seconds, the source voltage (V_S) drops from 230 V to

50.3 V and the series transformer injects a voltage (V_{Inj}) of 200 V so that the load voltage (V_L) remains constant at 256 V. During the duration of the sag voltage, the capacitance effect of the capacitor component able to store charge on the FL lamp load, causing the load voltage value to exceed the source voltage. In the disturbance conditions, the value of the source current (I_S) is 0.166 A and the load current (I_L) drops to 0.208 A. To keep the load voltage (V_L) maintain constant, BES releases its energy so that the DC link voltage ($V_{DC-Link}$) drops from 13.03 V to 7.33 V.

Fig. 8 shows a simulation curve voltage sag on a single-phase DVR system supplied by BES connects to the LED lamp load. At t = 1 to t = 2 seconds, the source voltage (V_S) drops from 230 V to 49.1 V and the series transformer injects a voltage (V_{Inj}) of 133 V so that the load voltage (V_L) remains constant at 185 V. During the disturbance conditions, the value of the source current (I_S) is 0.249 A, and the load current (I_L) increases to 0.789 A. To keep the load voltage (V_L) maintain constant, BES then releases its energy so that the DC link voltage ($V_{DC-Link}$) drops from 13.03 V to 8.06 V.

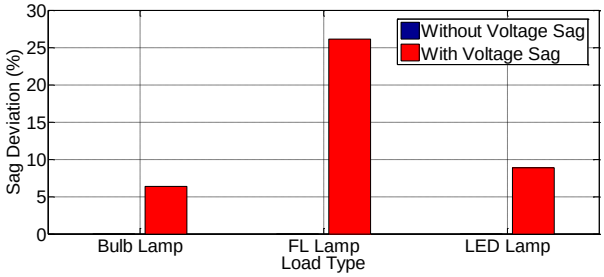

Figure. 9 Performance of sag deviation of V_L for single phase DVR-BES system on three load type

Fig. 9 shows that for the system without sag voltage, the series active filter circuit and series transformer on a single-phase DVR-BES system is not able to inject voltage into the load, so produces a percentage of sag deviation of load voltage (V_L)of 0%. Otherwise if the system with sag voltage, the single-phase DVR-BES system is able to maintain the load voltage (V_L) i.e. bulb lamp, FL lamp, and LED lamp of 216 V, 256 V, and 185 V, respectively. The percentage of load voltage deviation for the system with sag deviation of V_L for the three loads type are 6.4%, 26.13%, and 8.87%, respectively.

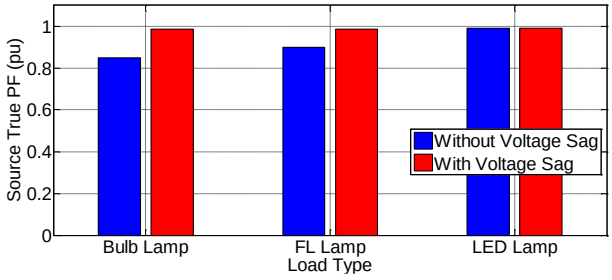

Figure.10 Performance of source true power-factor for single phase DVR-BES system on three load type

Fig. 10 shows the measurement of source true power-factor without voltage sag of the bulb lamp has the worst true power-factor (Pf_{true}) of 0.850 per-unit (pu) leading compared to an FL lamp of 0.900 pu leading and an LED lamp of 0.909 pu leading. Otherwise, for the system with voltage sag, the single-phase DVR-BES system produces source true power factor (Pf_{true}) for a bulb lamp, FL lamp, and LED lamp of 0.985 pu leading, 0.985 pu leading, and 0.990 pu leading respectively.

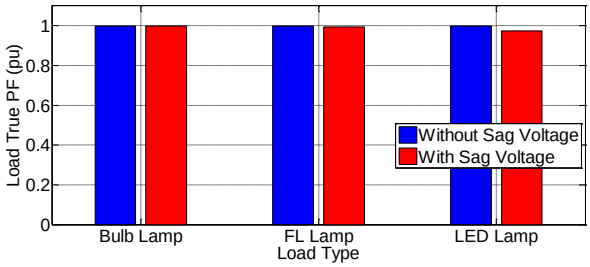

Figure. 11 Performance of load true power-factor for single phase DVR-BES system on three load type

Fig. 11 shows the measurement of load true power-factor without voltage sag for all load categories results in the same true power factor (Pf_{true}) of 0.999 pu leading. Otherwise, for the system with voltage sag is able to result in load true power factor (Pf_{true}) i.e. bulb lamp, FL lamp, and LED lamp of 0.975 pu leading, 0.998 pu leading, and 0.994 pu leading respectively.

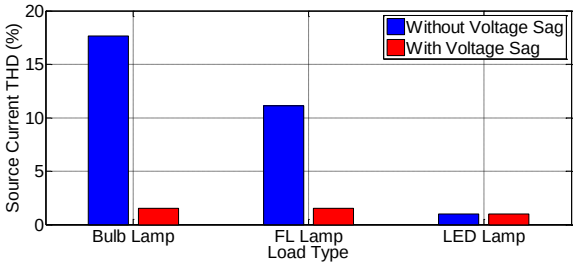

Figure. 12 Performance of source harmonics for single phase DVR-BES system on three load type

Fig. 12 shows that the system without sag voltage is able to produce the source THD_I for bulb lamp, FL lamp, and LED lamp of 17.647%, 11.111%, and 1.010% respectively. Otherwise, for the same system with sag voltage is able to result source THD_I. for bulb lamp, FL lamp, and LED lamp of 1.523%, 1.523%, and 1.010% respectively.

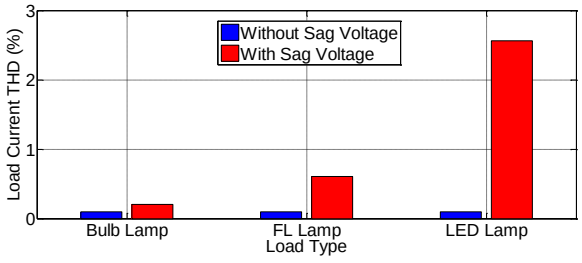

Figure. 13 Performance of load harmonics for single phase DVR-BES system on three load type

Fig. 13 shows that the system without voltage sag is able to produce the same load THD_I for bulb lamp, FL lamp, and LED lamp of 0.1001%. Otherwise, for the same system with voltage sag is able to result in load THD_I for bulb lamp, FL lamp, and LED lamp of 0.204%, 0.604%, and 2.564% respectively. Fig 10 and Fig. 11 shows in the case of voltage sag and three types of loads, the LHE lamp is able to result in the best performance because it is able to produce the highest source true power factor (Pf_{true}) of 0.990 pu and the lowest source THD_I of 1.010%. The source THD_I and load THD_I value in voltage sag also had met the IEEE 519.

Table 6. Comparison of implementation UVTG-DVR-BES-Arduino-Uno-LabVIEW (proposed study) and previous studies

No.	Authors	Methods	Depth Sag of V_S (%)	Sag Dev of V_L(%)	Load THD_V (%)	Source THD_I(%)	Source pf_{true}	Real Time
1	D.N. Katole, et.al [8]	Improved SRF	42	7.6	NA	NA	NA	Not
2	M.T. Hagh, et.al. [10]	FLC	92 without and 95 with DG	8.9 without DG and 6.4 with DG	1.26 without DG and 3.54 with DG	NA	NA	Not
3	H.K. Yada, et. al [16]	SOGI-PLL	30	3.0	NA	NA	NA	Not
4	S. Galeshi, et. al. [17]	Multilevel Cascade H-Bridge Inverter	20	0.0	4.0	NA	NA	Not
5	R. Nittala, et.al [19]	IDVR with VSI and CSI	27.7 with VSI and CSI	0 with VSI and CSI	0.06 with VSI and 0.05 with CSI	NA	NA	Not
6	E. Babaei, et. al. [22]	Direct Converter	65	0	7.07 (Average)	NA	NA	Not
7	A. Benhail, et.al. [23]	TDVR-PI	30	2.18	24	NA	NA	Not
8	J. Ye, et.al. [26]	Elliptical Restoration	60	NA	NA	NA	0.75	Not
9	R. Omar, et.al [28]	DVR-Super-capacitor	30	0	NA	2.38	NA	Not
10	C.K. Sundara-balan, et. al. [29]	CAESPDVR-ANFIS	46.67 (Average)	0.4	2.35	NA	NA	Not
11	V.K. Awaar, et.al. [31]	VSI-SPWM-NI-myRIO-1900-Labview	50	8.79	NA	NA	NA	Yes
12	A.Kiswantono et.al. [32]	UVTG-DVR-BES-PV	80	2.89 (Average)	5.81 (Average)	NA	NA	Not
13	**Proposed Study**	**UVTG-DVR-BES-Arduino-Uno-Labview**	**80**	**Bulb=6.4 FL =26.13 LED=8.87**	**NA**	**Bulb=1.523 FL=1.523 LED=1.010**	**Bulb=0.985 FL=0.985 LED=0.990**	**Yes**

Note: NA = note available

Table 6 shows the validation of the results for the proposed study compared to the 12 previous studies. The parameters observed are depth of sag of V_S, sag deviation of V_L, load THD_V, source THD_I, and real-time simulation. At [8], D.N. Katole, et.al proposed an improved SRF on the single-phase DVR series. With a depth of sag of V_S of 42%, this method produces a sag deviation of V_L of 7.6%. Furthermore, the FLC method for sag stress compensation was proposed by M.T. Hagh, et.al [10]. With a depth of sag of V_S of 92% without and 95% with DG, the FLC method yields a sag deviation of V_L of 8.9% without

DG and 6.4% with DG, and a load THD_V of 1.26% without DG and 3.54 with DG. The SOGI-PLL method proposed by Yada et. Al [16], with a depth of sag of V_S of 30% was able to produce a sag deviation of V_L of 3.0%. S. Galeshi, et. al [17] already offer Multilevel Cascade H-Bridge Inverter topology. With a depth of sag of V_S of 20%, this topology produces a sag deviation of V_L of 0% and a load of THD_V of 4%. IDVR configuration with VSI and CSI has been proposed by R. Nittala, et.al [19]. With a depth of sag of V_S of 27.7% (with VSI and CSI), this configuration resulted in a sag deviation of V_L of 0%, load THD_V of 0.06% (with VSI) and 0.05% (with CSI). E. Babaei, et. al [22] have proposed a direct converter topology to mitigate voltage sag. With a depth of sag of V_S of 65%, this topology produces a sag deviation of V_L of 0% and a load THD_V of 7.07% (average).

The TDVR-PI configuration has been proposed by A. Benhail, et.al. [23]. With a depth sag of V_S, of 30%, this configuration results in a sag deviation of V_L of 2.18% and a load THD_V of 24%. J. Ye, et.al [26] have proposed an elliptical restoration method for voltage sag compensation and power factor correction. With a depth of sag of V_S, of 60%, this method is able to produce a source pf_{true} of 0.75 pu. The DVR-Super-capacitor configuration has been implemented by R. Omar, et.al [28]. With a depth of sag of V_S, of 30%, this topology is able to produce a sag deviation of V_L of 0 % and source THD_I of 2.38%. The CAESPDVR-ANFIS topology has been investigated by C.K. Sundarabalan, et. al. [29]. With a depth of sag of V_S, of 46.67% (average), this topology was able to produce a sag deviation of V_L of 0.4% and a load of THD_V of 2.35%. V.K. Awaar, et.al. [31] have implemented a VSI-SPWM-based single-phase DVR model with the NI-myRIO-1900 interface monitored in real-time by LabVIEW. With a depth of sag of V_S, of 50%, this model was able to produce a sag deviation of V_L of 8.79%. DVR control supplied by BES-PV using the UVTG method has been observed by A. Kiswantono [32]. With a depth of sag of V_S, of 80%, this configuration and method were able to produce a sag deviation of V_L of 2.89% (average) and a load THD_V of 5.81% (average). Based on the results of research [31] and [32], then this study has implemented the single-phase DVR model using the UVTG method with the Arduino-Uno interface monitored in real-time by LabVIEW. With a depth of sag of V_S of 80%, the proposed model is able to produce sag deviation of V_L of 6.4% (Bulb), 26.13% (FL), and 8.87% (LED). The model is also able to produce THD_I source of 1.523% (Bulb), 1.523% (FL), and 1.101% (LED) and pf_{true} respectively 0.985% (Bulb), 0.985% (FL), and 0.909% (LED). The proposed study is able to give the best performance because it is able to produce source THD_I lower than [28] and source pf_{true} is higher than [26]. Another contribution is that by using the Arduino-Uno interface, the proposed model can be run and monitored in real-time with LabVIEW. It is different from the simulations conducted by 12 previous researchers (except [31]) which were still carried out off-line using Matlab/Simulink environment.

4. Conclusion

The system using a single-phase DVR supplied by BES with load voltage controlled by a UVTG method has been implemented. The model is connected to three types of linear/non-linear load i.e. bulb lamp, FL lamp, and LED lamp. This configuration is proposed to mitigate 80% voltage sag using the Arduino-Uno hardware and monitored by LabVIEW simulation in real-time. The investigated parameter are source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power-factor measurements are also carried out to obtain the harmonics of the source current and load current. During voltage sag, the single-phase DVR-BES system is able to maintain load voltage for all types of loads. From the system with voltage sag and three different types of loads, the LHE lamp is able to result in the best performance because it is able to produce the highest source current power factor (pf_{true}) and the lowest source THD_I. The source THD_I and load (THD_I) with voltage sag also had met the IEEE 519.

The proposed study is able to give the best performance because it is able to produce source THD_I lower than the previous studies. By using the Arduino-Uno interface, this model can be run and monitored in real-time with LabVIEW better from the simulations conducted by previous researchers which were still carried out off-line using Matlab/Simulink.

In a system using a single-phase DVR-BES connected to the FL load, there is a significant increase in load voltage of 256 V compared to the source voltage. The percentage of sag voltage for FL lamps also increased by 26.13% and has far exceeded the value of 5%. The implementation of a single-phase bidirectional inverter circuit as the interface between the BES and series active filters can be proposed as future work to overcome this problem. The measurement of source THD_V and load THD_V in the proposed model is also necessary to determine

the harmonic mitigation performance of the voltage within the IEEE 519 limit.

Conflicts of Interest

The authors declare no conflict of interest.

Author Contributions

Conceptualization, Y.A. Setiawan and A. Amirullah; methodology, Y.A. Setiawan and A. Amirullah; software, Y.A. Setiawan; validation, Y.A. Setiawan; formal analysis, Y.A. Setiawan and A. Amirullah; investigation, Y.A. Setiawan and A. Amirullah; resources, Y.A. Setiawan; data curation, Y.A. Setiawan; writing—original draft preparation, Y.A. Setiawan; writing—review and editing, Y.A. Setiawan; visualization, Y.A. Setiawan; supervision, A. Amirullah; project administration, Y.A. Setiawan; funding acquisition, A.Amirullah. All authors read and approved the final manuscript.

Acknowledgements

The authors would like to acknowledge to Institutions of Research and Community Service Universitas Bhayangkara Surabaya, for funding to this research base on Decree Letter Number 65/XI/2020/UBHARA date 19 November 2020.

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Received: November 24, 2020. Revised: January 22, 2021.

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Implementation of Single-Phase DVR-BES Based on Unit Vector Template Generation (UVTG) to Mitigate Voltage Sag Using Arduino Uno and Monitored in Real-Time Through LabVIEW Simulation

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Abstract: This paper aims to design and implement a single-phase dynamic voltage restorer (DVR) supplied by battery energy storage (BES) using load voltage controlled by the unit vector template generation (UVTG) method. The UVTG method on the DVR system is implemented using the Arduino-Uno hardware. LabVIEW-based interface simulation is used for monitoring the parameter in real-time during 80% voltage sag period i.e. source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power factor measurements are also carried out to obtain total harmonic distortion (THD) of the source current and load current. The single-phase DVR system is connected to load i.e. a 5-watt bulb lamp (linear-load), 5-watt fluorescent (FL) lamp (non-linear load), and 5-watt light-emitting diode (LED) lamp (non-linear load). During voltage sag, the single-phase DVR-BES system is able to maintain load voltage i.e. bulb lamp, FL lamp, and LED lamp of 216 volts, 256 volts, and 185 volts, respectively. The percentage of load sag voltage deviation for each load is 6.4%, 26.13%, and 8.87%, respectively. The measurement of source power-factor with voltage sag results in source true power factor of three loads of 0.985 pu leading, 0.985 pu leading, and 0.990 pu leading respectively. On the same system with voltage sag, single phase DVR-BES is able to result in source current THD for three loads of 1.523%, 1.523%, and 1.010% respectively. The proposed study is able to give the best performance because it is able to produce source current THD lower than the previous studies. By using the Arduino-Uno interface, this model can be run and monitored in real-time with LabVIEW better from the simulations conducted by previous researchers which were still carried out off-line using Matlab/Simulink.

Keywords: Single phase DVR, BES, Arduino uno, LabVIEW, Voltage sag.

1. Introduction

During the last decade, there has been an increase in the number of sensitive and critical loads. On the other hand, the use of these tools also has an impact on deteriorating Power Quality (PQ). Among a number of PQ problems, problems related to voltage mitigation are also of increasing importance from a sensitive load and customer point of view. PQ problems related to voltage i.e. voltage sag, voltage swell, voltage harmonics, fluctuations, interruptions, and imbalance. In accordance with IEEE 1346 [1] and IEEE 1159 [2] standards, the sag voltage is defined as the RMS (root mean square) AC voltage sag with a magnitude of 10% to 90% of the nominal voltage, at power frequencies with a duration of 0.5 cycles to one minute. The voltage sag is caused by a single-phase short circuit to ground in the power system, starting in large-capacity induction motors, and sudden changes in the system connected to large loads [3]. Viewed from the system, the DVR is divided into two systems, namely one-phase DVR and three-phase DVR. Then three-phase DVR is connected to a 3 phase 3 wire (3P3W) or a 3 phase 4 wire (3P4W) system. Next, this paper will further focus on the design and implementation of single-phase DVRs to mitigate voltage sag at the source side and connect to a number of the linear/non-linear load. The simulation of low voltage single phase DVR based on the multilevel inverter to protect sensitive

loads has been implemented in [4]. The proposed model is able to compensate for the voltage sag and increase the PQ on the load side. A DVR topology using a cascaded multilevel direct pulse with modulation (PWM) ac-ac converter has been proposed in [5]. In this scheme, the unit cell of the multilevel converter consists of a single-phase ac-ac converter PWM using a switching cell (SC) structure that is paired with an inductor. The implementation of the phase shift PWM technique is capable of significantly reducing the size of the output filter inductor. One and three-phase DVR control schemes using PSCAD/EMTDC have been observed in [6]. The proposed system is able to compensate for a number of voltage sag variations and keep the load voltage constant. DVR control scheme with an ac-ac converter, based on voltage drop characterization has been investigated in [7] to reduce voltage drop with phase jumps. The superiority of the proposed control scheme is then validated on an ac-ac interphase converter topology. The vector-based one-phase DVR control using an improved synchronous reference frame (SRF) has been proposed in [8]. The vector analysis used in this control method during the voltage period was able to provide the magnitude and phase of the injection voltage.

The control methods to reduce sag voltages using a fuzzy logic controller (FLC) connected with sensitive loads [9] and distributed generation (DG) [10] have been proposed. The FLC control was used to generate pulses with the Sinusoidal Pulse Width Modulation (SPWM) technique at the output of an active filter circuit. Comparing to proportional-integral (PI) control, FLC control was able to provide better performance during voltage sag because it has more advantages in terms of resistance to parameter variations and system execution. A DVR with DG-connected FLC control also able to enhance voltage profiles, power quality, and reliability. Single-phase and three-phase DVRs use a single-phase ac to ac matrix converter to replace voltage source inverter (VSI), has been investigated by Matlab in [11, 12], and in PSCAD [13], at a number of variations in source voltage (sag, flicker, and unbalance). The single-phase DVR has been simulated in [14] and a special voltage detection method for single-phase DVRs has been introduced in [15]. The simulation results show that the DVR was able to maintain the nominal load voltage, despite interference and other abnormal conditions from the source side. The special detection method using double closed-loops of the proportional-resonant controller was also able to provide superior performance in voltage detection and compensation.

The DVR control scheme for reference voltage generation based on a single-phase Second Order Generalized Integrator-Phase Lock Loop (SOGI-PLL) using a series of active compensator has been observed in [16]. The proposed scheme is capable of dynamically responding, detecting, and rapidly compensating for sag/swell voltages without and with phase jumps. A DVR that uses a multilevel H-bridge inverter with a capacitor as an energy source has been introduced in [17]. This configuration allows the DVR to connect directly to a medium-voltage network, eliminating the need for a series injection transformer and batteries. The DVR model was the same but uses a single H-Bridge inverter and a battery on sag/swell voltage disturbances connected to the non-linear load which has also been observed in [18]. Interline DVR (IDVR) on two same [19] and different voltage distribution lines with voltage source inverter (VSI) and current source inverter (CSI) [20] to restore voltage sag and harmonics has been introduced. When voltage sag and voltage distortion occur on one channel, the DVR on the same channel is able to perform voltage compensation and harmonics elimination, while the other DVR can recharge the energy to the DC-link to maintain the DC-link voltage constant.

In order to efficiently the number of equipment in the DVR circuit configuration, the implementation of a direct ac/ac converter on the DVR has been introduced in [21, 22]. The proposed configuration uses the minimum switches, did not require a dc-link energy storage element, and has a longer compensation time during sag/swell voltage disturbances. The compensation voltage for each phase is taken from each of the three-phase sources so that each converter was able to operate independently and is also able to compensate for single-phase blackouts and unbalance sag/swell voltages. The use of a single-phase transformer-less DVR (TDVR) to mitigate the sag/swell voltage has been observed in [23]. The proposed configuration was capable of reducing system size and losses compared to DVR which using a series transformer. The single-phase interactive channel DVR using the sag voltage detection algorithm has been developed in [24]. The detection algorithm has a hybrid structure consisting of a momentary detection section and a RMS variation detection section. The DVR development could compensate for input voltage sag or interrupt in 2.0-ms delay and can be used effectively for sensitive loads.

The single-phase DVR with synchronous reference frame control under distorted source conditions has been applied in [25]. The proposed control using a moving average filter (MAF) is

capable of extracting positive sequence fundamental components as well as being able to mitigate voltages sag and distorted source voltages. The single-phase DVR using elliptical restoration-based voltage compensation to correct the power factor on the source side has been proposed in [26]. The active and reactive voltage components and centrifugal angles are used to formulate an elliptical compensation path. So that the voltage will be in-phase with the load current using precise control of the DVR injection voltage. The optimization of the voltage injection technique in DVR to protect sensitive loads has been observed in [27]. The recursive least square (RLS) method is used to estimate the magnitude and phase of the voltage in order to minimize the amplitude of the injection voltage. Meanwhile, repetitive control was proposed to track the compensation voltage. Both controls are suitable for sinusoidal reference and are reliable for mitigating harmonics, sags, and swell distortions.

Energy storage in single or three-phase DVR circuits related to the capacity and type of energy storage has become the attention of many researchers. The determination of the two parameters relates to the ability and duration of the energy storage to supply real power to the inverter during a fault. Unbalanced voltage compensation in 3P3W system using DVR using a super capacitor has been investigated in [28]. The proposed DVR configuration uses a control based on the d-q-0 and Proportional Integral (PI) transformation technique and is further coded using a digital signal processor (DSP). DSP control and super capacitor implementation can mitigate unbalanced voltage disturbances. A compressed air energy storage powered dynamic voltage restorer (CAESPDVR) with ANFIS control has been proposed in [29] to compensate for unbalanced sag/swell voltages and harmonics. The single-phase DVR configuration using a hybrid energy storage system (HES) has been developed in [30].

The HES series consists of superconducting magnetic energy storage (SMES) in collaboration with battery energy storage (BES) on a DC type DVR. The proposed HES concept integrated with fast response large power SMES unit and low-cost high capacity BES can further be implemented in large scale DVR development. The DVR uses VSI method with SPWM to compensate for sag voltage has been implemented in [31]. The voltage sag was able to be simulated and monitored by LabVIEW with the NI myRIO-1900 interface using LabVIEW in real-time. The mitigation of sag/swell voltage and harmonics in low voltage distribution networks using DVR-BES-PV using the UVTG control method has been observed in [32]. The proposed model was able to compensate for sag voltage between 10% to 90% and swell voltage between 110% to 180% with a voltage THD within the IEEE 519 limit.

In this paper, BES is proposed as energy storage and implemented in single-phase DVR using load voltage control with the UVTG method and connected to linear/non-linear loads. The UVTG method on the DVR system is implemented using the Arduino-Uno microcontroller hardware. The LabVIEW based interface simulation is used to monitor electrical quantities in real-time during the voltage sag period i.e. source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power factor measurements are also carried out to obtain the total harmonic value or Total Harmonic Distortion (THD) of the source current and load current.

This paper is arranged as follows. Section 2 presents the proposed method, UVTG method, percentage of voltage sag, true power factor and harmonic, single-phase DVR-BES using LabVIEW, as well as hardware and software implementation, Section 3 presents results and discussion of the source voltage, injection voltage, load voltage, DC-link voltage, source current, load current, percentage of

Table 1. Abbreviation

Symbol	Description
PQ	Power Quality
DVR	Dynamic Voltage Restorer
BES	Battery Energy Storage
PV	Photovoltaic
UVTG	Unit Vector Template Generation
THD	Total Harmonic Distortion
Pf_{true}	True Power Factor
FL	Fluorescent
LED	Light Emitting Diode
DG	Distributed Generation
3P3W	Three Phase Three Wire
3P4W	Three Phase Four Wire
SPWM	Sinusoidal Pulse Width Modulation
VSI	Voltage Source Inverter
CSI	Current Source Inverter
SOGI-PLL	Second Order Generalized Integrator-Phase Lock Loop
CAESPDVR	Compressed Air Energy Storage Powered Dynamic Voltage Restorer
ANFIS	Artificial Intelligent Fuzzy Inference System
IDVR	Interline Dynamic Voltage Restorer
CB	Circuit Breaker
RMS	Root Mean Square
GUI	Graphic User Interface
PC	Personal Computer
USB	Universal Serial Bus
PU	Per Unit

voltage sag, true power-factor, and current THD which analyzed from data measured by Arduino-Uno and monitored by LabVIEW. In this section, the system connected to the linear/non-linear load with and without voltage sag is selected to present the best performance single-phase DVR-BES system connected to three different types of load during voltage sag. Finally, this paper is concluded in Section 4. All manuscripts must be in English. These guidelines include complete descriptions of the fonts, spacing, and related information for producing your proceedings manuscripts. Table 1 shows the abbreviations used in this paper.

2. Research method

2.1 Proposed method

Fig. 1 shows a single-phase DVR supplied by BES using load voltage control with the UVTG method. The DVR is a tool that functions to compensate for the load voltage in the event of a voltage sag disturbance on the source bus at a level of 0.1 to 0.9 per unit. The UVTG method on the DVR system is implemented using the Arduino-Uno hardware. LabVIEW-based interface simulation is used to monitor electrical quantities in real-time during the voltage sag period.

The observed parameters are source voltage (V_S), injection voltage (V_{inj}), load voltage (V_L), DC-link voltage ($V_{DC-Link}$), source current (I_S), and load current (I_L). The true power-factor (Pf_{true}) measurements are also carried out to obtain the THD value of the source current and load current. There are two cases in this study, the source without voltage sag, and with an 80% voltage sag. In each case, the single-phase DVR system is supplied by BES connected to a 5-watt bulb lamp (linear load), 5 watt FL lamp (non-linear load), and 5 watts LED lamp (non-linear load), so the total selected case is six. The CB1, CB2, and CB3 are used to connect and disconnect links to three linear/non-linear loads. The DVR-BES system configuration is then run based on a predetermined case using Arduino-Uno microcontroller interfaced communication and the results are simulated and monitored in real-time by a LabVIEW. Table 2 shows the notation list and parameters of Fig. 1.

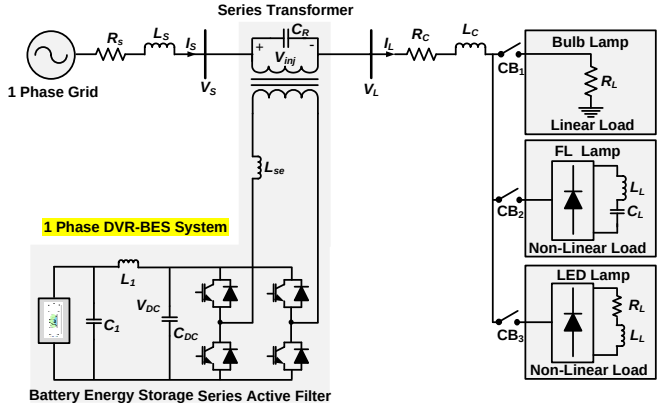

Figure. 1 Proposed single phase DVR-BES connected to linear/non-linear load

V_S	Source Voltage
V_{inj}	Injection Voltage
V_L	Load Voltage
$V_{DC-Link}$	DC-Link Voltage
I_S	Source Current
I_L	Load Current
I_L^*	Reference Load Voltage
V_m	Peak Fundamental Input Voltage Magnitude
K	Gain
S_1, S_2, S_3, S_4	Gating Signal 1, 2, 3, and 4
Sag_{dev}	Voltage Sag Deviation
$V_{pre-sag}$	Pre-Sag Voltage
V_{sag}	Sag Voltage
Pf_{true}	True Power Factor
P_{avg}	Average Power
S	Apparent Power
V_{rms}	RMS Voltage
I_{rms}	RMS Current
V_{1rms}	RMS Fundamental Voltage
I_{1rms}	RMS Fundamental Current
THD_V	Voltage THD
THD_I	Current THD
P_{1avg}	Fundamental Average Power
$Pf_{displacement}$	Displacement Power Factor
$Pf_{distorted}$	Distorted Power Factor
R_S	Line Resistance (0.1 ohm)
L_S	Line Inductance (0.15 mH)
R_C	Load Resistance (0.4 ohm)
L_C	Load Inductance (15 mH)
L_{Se}	Series Inductance (0.015 mH)
L_1	BES Inductance (6 mH)
C_1	BES Capacitance (1000 µF)
C_{DC}	DC-Link Capacitance (200 µF)
R_L	Linier/Non-Linear Resistance (0.6 ohm)
L_L	Non-Linear Load Inductance (0.15 mH)
C_L	Non-Linear Load Capacitance (3.3 µF)
C_R	Ripple Capacitance (0.2 µF)

Table 2. Notation list and parameters

Notation	Description

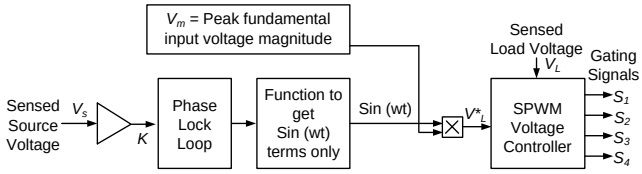

Figure. 2 UVTG control on single phase series active filter

2.2 Unit voltage template generation method

The series active filter protect sensitive loads against several voltage disturbances from the source bus. In [31], the control method of source and load voltage in a three-phase series active filter has been discussed. Using the same procedure, the authors propose the same method for single-phase series active filter control as shown in Fig. 2. This method extracts UVTG from the distorted input supply. Then, the template is expected to be an ideal sinusoidal signal with a unity amplitude. The source of the distorted voltage is measured and divided by the peak amplitude fundamental input voltage (V_m).

A single-phase locked loop (PLL) is used in order to generate sinusoidal unit vector templates with a phase lagging by the use of the sine equation. The reference signal of the load voltage is calculated by multiplying the unit vector templates with the peak amplitude of the fundamental input voltage (V_m). The reference load voltage (V_L^*) is then compared to the sensed load voltage (V_L) by a SPWM controller used to generate the desired four gating signal on a single-phase series active filter.

2.3 Percentage of voltage sag deviation

The recommended standard of practice on monitoring voltage sag/swell as part of electric power quality parameters is IEEE 1159 [2]. This standard presents the definition and table of voltage sag base on categories (instantaneous, momentary, temporary) typical duration, and typical magnitude. The percentage of load voltage sag deviation is formulated in Eq. (1) [31].

$$Sag_{dev}(\%) = \frac{|Vpre\_sag - V\_sag|}{Vpre\_sag} \quad (1)$$

2.4 True power factor and harmonics

The true power factor at the load is defined as the ratio of average power to apparent power. The true power factor for both sinusoidal and non-sinusoidal situations is presented in Eq. (2) [33].

$$pf_{true} = \frac{P_{avg}}{S} = \frac{P_{avg}}{V_{rms}\, I_{rms}} \quad (2)$$

$$V_{rms} = V_{1rms}\sqrt{1 + (THD_V/100)^2} \quad (3)$$

$$I_{rms} = I_{1rms}\sqrt{1 + (THD_I/100)^2} \quad (4)$$

By substituting Eq. (3) and Eq. (4) into Eq. (2), the true power factor (Pf_{true}) results in Eq. (5) for both sinusoidal and non-sinusoidal cases [33].

$$pf_{true} = \frac{P_{avg}}{V_{1rms}\, I_{1rms}\sqrt{1+(THD_V/100)^2}\sqrt{1+(THD_I/100)^2}} \quad (5)$$

A useful simplification can be made by expressing Eq. (5) as a product of two components defined in Eq. (6).

$$pf_{true} = \frac{P_{avg}}{V_{1rms}\, I_{1rms}} \times \ldots \ldots \frac{1}{\sqrt{1+(THD_V/100)^2}\sqrt{1+(THD_I/100)^2}} \quad (6)$$

By making the following two assumptions: (1) In most cases, the contributions of harmonics above the fundamental to average power are very small, so that is $P_{avg} \approx P_{1avg}$ and (2) Since THD_V is less than 10%, then from (12) we see that $V_{rms} \approx V_{1rms}$. Then, merging both assumptions into Eq. (6) results in the following approximate function for the true power factor (Pf_{true}) presented in Eq. (7) [33].

$$pf_{true} = \frac{P_{1avg}}{V_{1rms}\, I_{1rms}} \times \frac{1}{\sqrt{1+(THD_I/100)^2}} = Pf_{displacement} \times Pf_{distorted} \quad (7)$$

Because displacement power factor (Pf_{disp}) could never be greater than unity, Eq. (7) shows that the true power factor (Pf_{true}) in non-sinusoidal cases has the upper limit so finally its function is defined in Eq. (8) [33].

$$pf_{true} \leq Pf_{distorted} = \frac{1}{\sqrt{1+(THD_I/100)^2}} \quad (8)$$

2.5 Single phase DVR-BES using labVIEW

The implementation of the single-phase DVR-BES system consists of several stages. That stage i.e. create a single-phase series active filter, create a gate driver to trigger the MOSFET in the series active filter, create a SPWM program to drive the gate driver as an inverter trigger and create a monitoring program in LabVIEW. Fig. 3 presents a schematic diagram of a single phase DVR-BES system.

Fig. 3 shows that the BES and series active filters play an important role in compensating for the

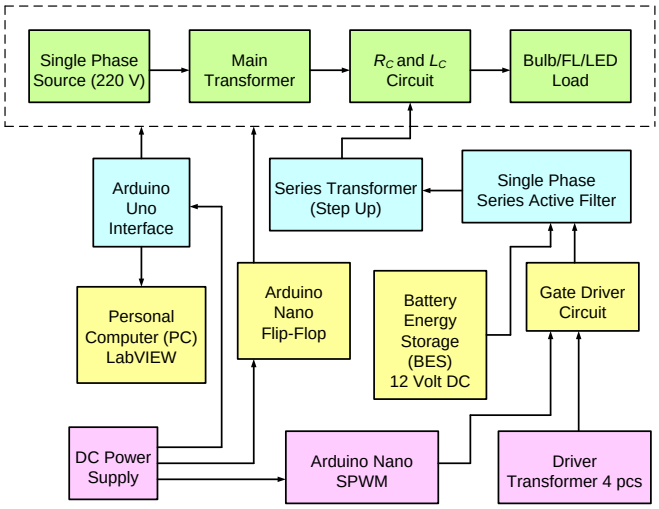

Figure. 3 A schematic diagram of single phase DVR-BES

voltage sag on a single-phase DVR. The step-up transformer that is installed in a series against the load functions to inject the voltage from the series active filter to the load. The main energy source for series active filters uses BES DC voltage 12 V with a capacity of 7.2 Ah. The process of changing the DC to AC voltage begins with the Arduino Nano SPWM microcontroller providing Sinusoidal SPWM pulses to the Gate Driver circuit which has the main component of the TLP 250 Optocoupler IC, then the Gate Driver circuit triggers the IRFP250 MOSFET gate on a series active filter circuit cross-like as an electric current cycle in the circuit bridge diode rectifier. So that it will produce an AC output from a series active filter circuit. The output voltage of the series active filter is an AC voltage of 7 V depending on the battery voltage conditions, which will then be increased to an AC voltage of 220 V using a step-up transformer. The step-up series transformer has a power of 600 VA with a primary AC input voltage of 7.2 V and a secondary AC output voltage of 220 V. The goal is that the series active filter is able to inject enough power to compensate for the sag voltage at a level of 10% to 90%.

The Arduino Nano flip-flop functions as a timer to run system simulations using a single-phase DVR-BES without and with sag voltage. The Arduino nano has been programmed with a flip-flop program with the 1-second case instructing the relay to turn "on" as a representation of the system experiencing sag voltage and 1 second ordering the relay to turn "off" as a representation of the system without experiencing sag voltage. This timer is expected to function when there is a sag voltage and automatically orders a single-phase active filter to inject a voltage compensation into the load so that the load voltage will remain stable.

The Arduino Uno interface functions as a medium for receiving data from voltage sensors and current sensors that are measuring the amount of electricity in the DVR circuit and sending the data to a personal computer (PC) with LabVIEW software. Curves and data displayed in LabVIEW i.e. source voltage, load voltage, injection voltage, DC-link voltage, source current, and load current respectively. The display form implemented in LabVIEW is in the form of graphs and number indicators. With a graphic display, the reader will find it easier to observe the wave condition both voltage and current during the system condition without and with voltage sag. All data displayed in LabVIEW is real-time and continuous data as long as the single-phase DVR-BES system is operated to the system. In addition to using the LabVIEW, data collection is also carried out by the cos-phi meter to determine the value of the true power factor of source and load as a basis for determining the harmonic of source and load currents. The single-phase DVR-BES system connected to three linear/non-linear loads i.e. bulb lamp 5 W (linear), FL lamp 5 W (non-linear), LED lamp 5 W (non-linear) respectively.

2.5 Hardware and software implementation

The LabVIEW interface software diagram consists of the main program in the form of a Graphic User Interface (GUI) which functions to run all indicators and controls on the front panel. Fig. 4 shows the model of the single-phase DVR-BES hardware circuit. The nominal parameters of Fig. 4 are presented in Table 3.

Table 3. Nominal of device parameters

Devices	Design Values
Single phase source voltage	220 V
Frequency	50 Hz
Series Transformer (*step-up)*	600 VA 7,2/220 V
Main Transformer (CT)	3 A
Current Sensor ACS 712	5A
Relay	1 device
Arduino Uno (Interface)	1 device
Arduino Nano (Flip-Flop)	1 device
Arduino Nano (SPWM))	1 device
Load Resistance (R_C)	0.4 ohm
Load Inductance (L_C)	15 mH
Cos-phi-Meter	1 device
Battery Energy Storage (BES)	12 V/7.2 Ah
DC-link Capacitance (C_{DC})	1000 μF
Bulb Lamp Load	5 W
FL Lamp Load	5 W
LED Lamp Load	5 W

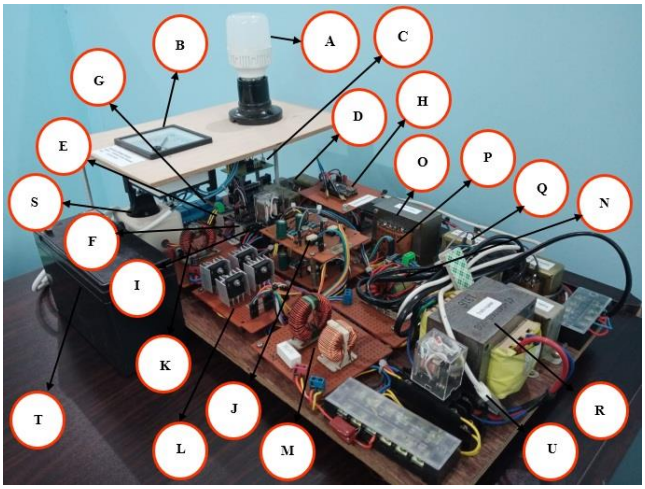

Figure. 4 Single-phase DVR-BES hardware

Where A: Load; B: Cos-phi-meter; C: Arduino Uno; D: Voltage Sensor Transformer; E: Current Sensor; F: Arduino Nano SPWM; G: Relay 1 (4 Channel); H: Arduino Nano Flip-Flop; I: Two Relays (220V-AC); J: Gate Driver Optocoupler; K: DC-link Capacitance and BES filter (C_{DC}, L_1, C_1); L: Series Active Filter; M: Load Impedance (R_C, L_C); N: Series Inductance (L_{Se}); O: Main Transformer; P: Source Current Sensor; Q: Gate Driver Transformer; R: Series Transformer; S: Source Voltage; T: BES and U: Universal Serial Bus (USB) for data communication between hardware PC.

Fig. 5 shows the overall GUI program design and the component parts of the single-phase DVR-BES. In order for the LabVIEW software interface on the PC to communicate with the Arduino Uno, a program is needed to communicate the two devices. The communication program used by Lifa Base. Lifa Base is the driver for Arduino Uno in connecting data communication with PC. Lifa Base is the default program from Arduino when users install LabVIEW.

3. Results and discussion

Fig. 1 shows a series of DVR supplied by BES connected to a load of Bulb, FL, and LED respectively. The series transformer connected to the load functions to inject the voltage from the series active filter during voltage sag. The Arduino Nano Flip-Flop is used as a timer to run simulated data collection. The cycle timer applied to the DVR is 1 second on and 1 second off. The data collection period is carried out with a LabVIEW simulation for 3 seconds, with 80% depth of source voltage sag duration between 1 to 2 seconds. Data collection is carried out at 1.5 seconds from the curve of the source voltage (V_S), injection voltage (V_{inj}), load voltage (V_L), DC-link voltage ($V_{DC-Link}$), source current (I_S), and load current (I_L), curves. The true power-factor (Pf_{true}) data in the source bus and load bus is measured from the cos-phi meter.

Using the same LabVIEW simulation procedure and period, data collection is also carried out without the voltage sag. The percentage of load voltage sag deviation is calculated using Eq. (1) with a pre-sag voltage of 203 V. Base on true power-factor, then harmonics current is measured using Eq. (8). Table 4 presents the performance of voltage, current, and percentage of sag deviation of load voltage (V_L) of the single-phase DVR supplied by BES without and with voltage sag disturbance. Table 5 presents the performance of true power factor (Pf_{true}) and harmonics value of the single-phase DVR supplied by BES without and with voltage sag disturbance. Fig. 6, Fig. 7, and Fig. 8 show the performance of voltage and current of the single-phase DVR supplied by BES connecting to bulb lamp, FL lamp, and LED lamp load respectively.

Fig. 6 shows the simulation curve of the sag voltage on a single-phase DVR system supplied by a BES connected to a bulb lamp load. The voltage sag disturbance lasts from t = 1 to t = 2 seconds with a total simulation time of 3 seconds. The measurements on all simulation parameters curves are carried out at t = 1.5 seconds. At t = 1 to t = 2 seconds, the source voltage (V_S) drops from 230 V to 44.7 V, and the series transformer injects a voltage (V_{Inj}) of 168 V so that the load voltage (V_L) remains constant at 216 V. In this disturbance condition the value of the source current (I_S) is 0.228 A and the load current (I_L) drops to 0.45 A. To keep the load voltage (V_L) maintain constant, BES releases its energy so that the DC link voltage ($V_{DC-Link}$) drops from 13.03 V to 8.20 V.

Fig. 7 shows the simulation curve of sag voltage on a single-phase DVR system supplied by the connected BES to the FL lamp load. At t = 1 to t = 2 seconds, the source voltage (V_S) drops from 230 V to 50.3 V and the series transformer injects a voltage (V_{Inj}) of 200 V so that the load voltage (V_L) remains constant at 256 V. During the duration of the sag voltage, the capacitance effect of the capacitor component able to store charge on the FL lamp load, causing the load voltage value to exceed the source voltage. In the disturbance conditions, the value of the source current (I_S) is 0.166 A and the load current (I_L) drops to 0.208 A. To keep the load voltage (V_L) maintain constant, BES releases its energy so that the DC link voltage ($V_{DC-Link}$) drops from 13.03 V to 7.33 V.

Fig. 8 shows a simulation curve voltage sag on a single-phase DVR system supplied by BES connects to the LED lamp load. At t = 1 to t = 2 seconds, the

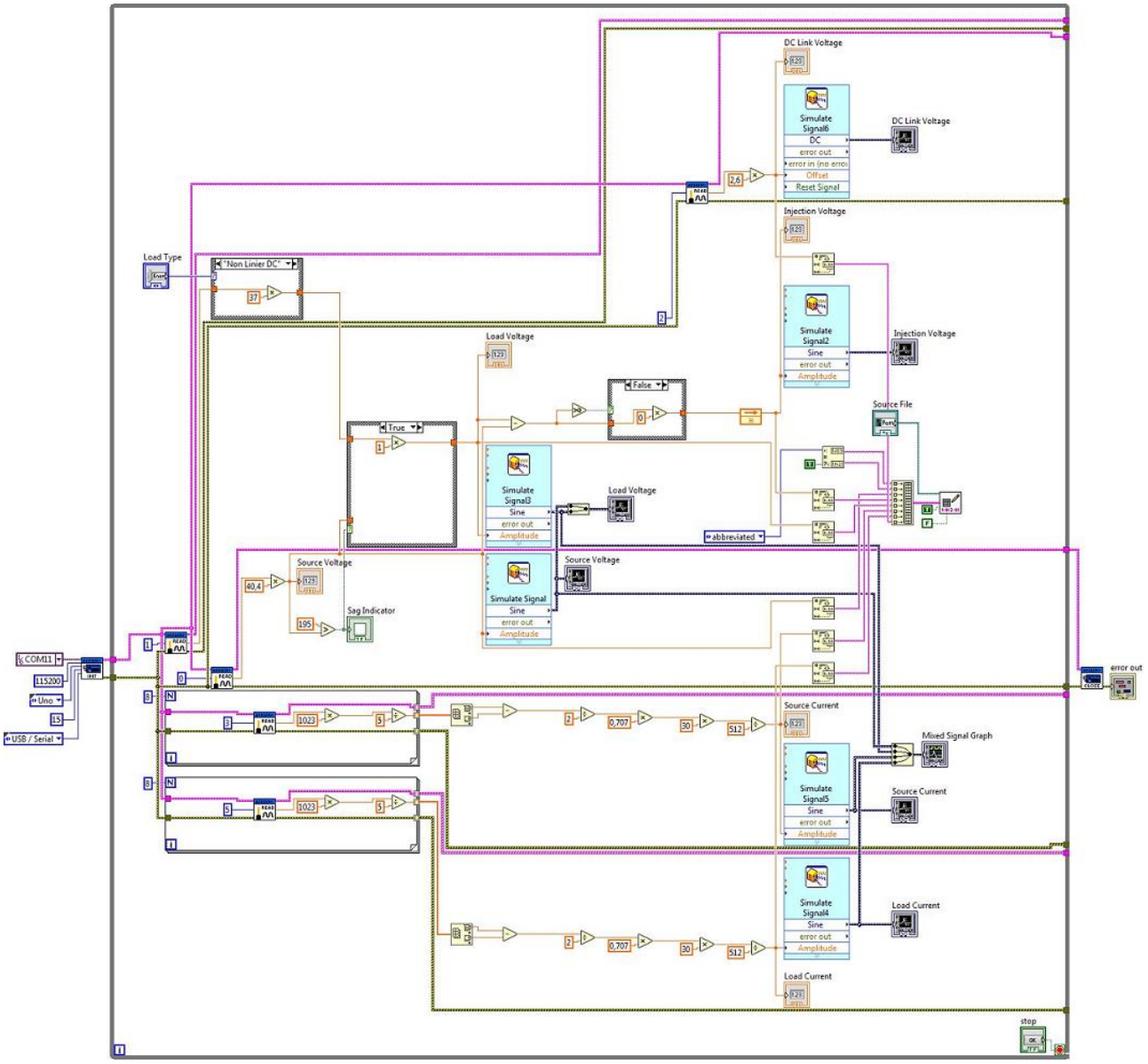

Figure. 5 Software design using LabVIEW interface for simulate signal i.e. (A) arduino-uno data communication, (B) source voltage (V_S), (C) injected voltage (V_{Inj}), (D) load voltage (V_L), (E) source current (I_S), (F) load current (I_L), (G) DC-link voltage ($V_{DC-Link}$), and (H) mixed signal graph

Table 4. Performance of voltage, current, and sag deviation of load voltage of the single-phase DVR supplied by BES

No.	Load Type	V_S (V)	$V_{Inj}(V)$	V_L (V)	I_S (A)	I_L (A)	$V_{DC-Link}$ (V)	Sag Dev of V_L (%)
Without Voltage Sag								
1.	Bulb Lamp	203	0	203	0.208	0.166	13.03	0
2.	FL Lamp	203	0	203	0.208	0.083	13.03	0
3.	LED Lamp	203	0	203	0.270	0.166	13.03	0
With Sag Voltage								
4.	Bulb Lamp	44.7	168	216	0.228	0.145	8.20	6.40
5.	FL Lamp	50.3	200	256	0.166	0.208	7.33	26.13
6.	LED Lamp	49.1	133	185	0.249	0.789	8.06	8.87

source voltage (V_S) drops from 230 V to 49.1 V and the series transformer injects a voltage (V_{Inj}) of 133 V so that the load voltage (V_L) remains constant at 185 V. During the disturbance conditions, the value of the source current (I_S) is 0.249 A, and the load current (I_L) increases to 0.789 A. To keep the load voltage (V_L) maintain constant, BES then releases its energy so that the DC link voltage ($V_{DC-Link}$) drops

Table 5. Performance of power factor and harmonics of the single-phase DVR supplied by BES

No.	Load Type	Source Pf_{true} (pu)	Load Pf_{true} (pu)	Source THD_I (%)	Load THD_I (%)
Without Voltage Sag					
1.	Bulb Lamp	0.850	0.999	17.647	0.1001
2.	FL Lamp	0.900	0.999	11.111	0.1001
3.	LED Lamp	0.990	0.999	1.010	0.1001
With Sag Voltage					
4.	Bulb Lamp	0.985	0.998	1.523	0.2040
5.	FL Lamp	0.985	0.998	1.523	0.6040
6.	LED Lamp	0.990	0.975	1.010	2.5640

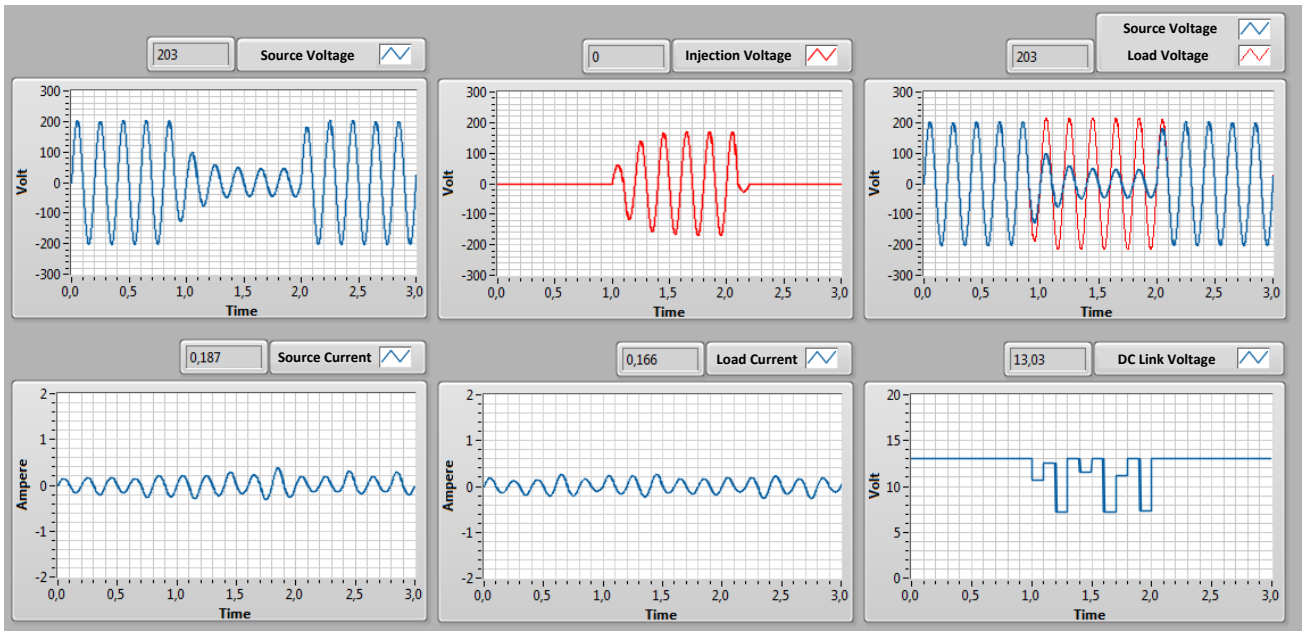

Figure. 6 Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to bulb lamp load using LabVIEW

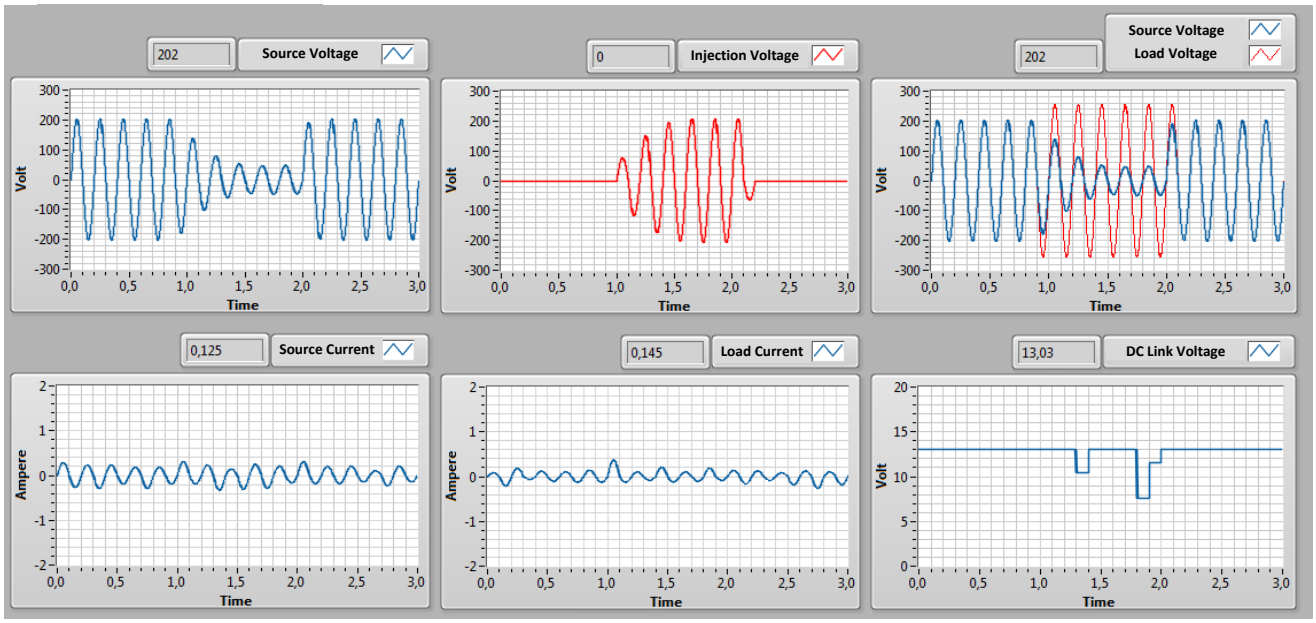

Figure. 7 Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to FL lamp load using LabVIEW

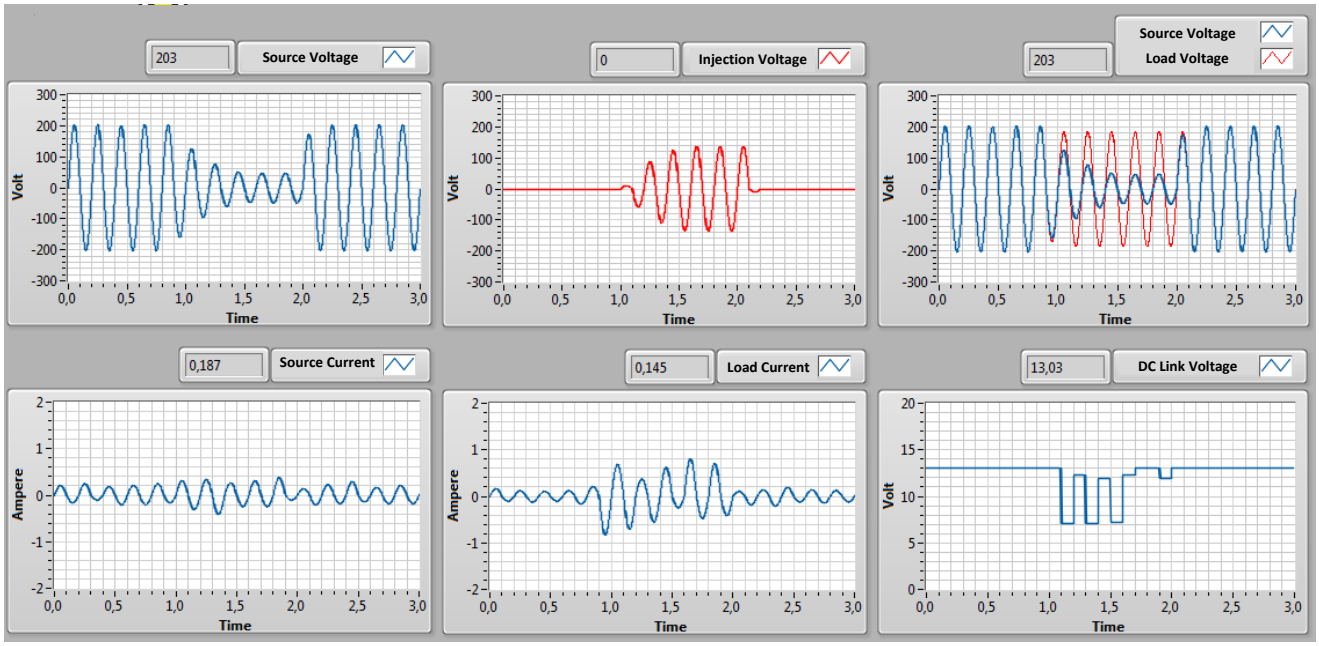

Figure. 8 Performance of V_S, V_{Inj}, V_L, I_S, I_L, and $V_{DC-Link}$ from the single-phase DVR- BES connected to LED lamp load using LabVIEW

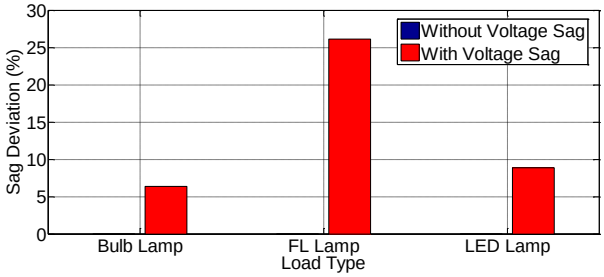

Figure. 9 Performance of sag deviation of V_L for single phase DVR-BES system on three load type

from 13.03 V to 8.06 V.

Fig. 9 shows that for the system without sag voltage, the series active filter circuit and series transformer on a single-phase DVR-BES system is not able to inject voltage into the load, so produces a percentage of sag deviation of load voltage $(V_L)$of 0%. Otherwise if the system with sag voltage, the single-phase DVR-BES system is able to maintain the load voltage (V_L) i.e. bulb lamp, FL lamp, and LED lamp of 216 V, 256 V, and 185 V, respectively.

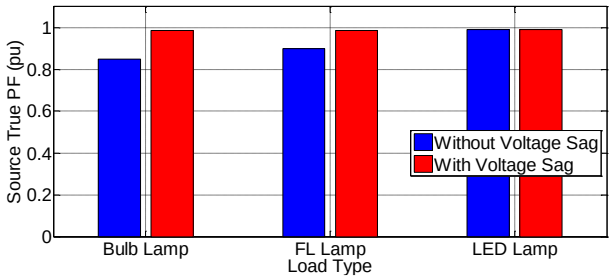

Figure. 10 Performance of source true power-factor for single phase DVR-BES system on three load type

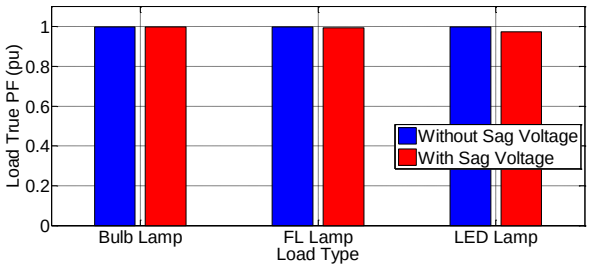

Figure. 11 Performance of load true power-factor for single phase DVR-BES system on three load type

The percentage of load voltage deviation for the system with sag deviation of V_L for the three loads type are 6.4%, 26.13%, and 8.87%, respectively.

Fig. 10 shows the measurement of source true power-factor without voltage sag of the bulb lamp has the worst true power-factor (Pf_{true}) of 0.850 per-unit (pu) leading compared to an FL lamp of 0.900 pu leading and an LED lamp of 0.909 pu leading. Otherwise, for the system with voltage sag, the single-phase DVR-BES system produces source true power factor (Pf_{true}) for a bulb lamp, FL lamp, and LED lamp of 0.985 pu leading, 0.985 pu leading, and 0.990 pu leading respectively.

Fig. 11 shows the measurement of load true power-factor without voltage sag for all load categories results in the same true power factor (Pf_{true}) of 0.999 pu leading. Otherwise, for the system with voltage sag is able to result in load true power factor (Pf_{true}) i.e. bulb lamp, FL lamp, and LED lamp of 0.975 pu leading, 0.998 pu leading, and 0.994 pu leading respectively.

Fig. 12 shows that the system without sag voltage

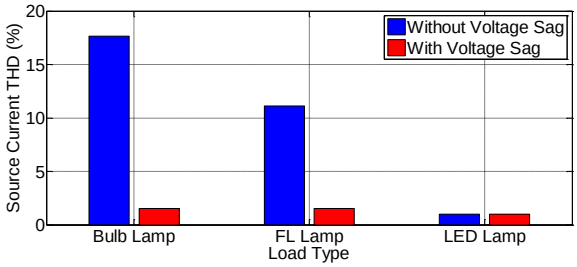

Figure. 12 Performance of source harmonics for single phase DVR-BES system on three load type

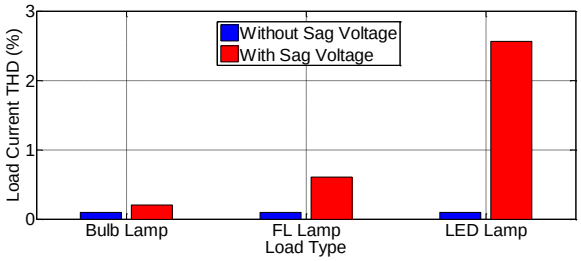

Figure. 13 Performance of load harmonics for single phase DVR-BES system on three load type

Table 6. Comparison of implementation UVTG-DVR-BES-Arduino-Uno-LabVIEW (proposed study) and previous studies

No.	Authors	Methods	Depth Sag of V_S (%)	Sag Dev of V_L(%)	Load THD_V (%)	Source THD_I(%)	Source pf_{true}	Real Time
1	D.N. Katole, et al [8]	Improved SRF	42	7.6	NA	NA	NA	Not
2	M.T. Hagh, et al. [10]	FLC	92 without and 95 with DG	8.9 without DG and 6.4 with DG	1.26 without DG and 3.54 with DG	NA	NA	Not
3	H.K. Yada, et. al [16]	SOGI-PLL	30	3.0	NA	NA	NA	Not
4	S. Galeshi, et al. [17]	Multilevel Cascade H-Bridge Inverter	20	0.0	4.0	NA	NA	Not
5	R. Nittala, et al [19]	IDVR with VSI and CSI	27.7 with VSI and CSI	0 with VSI and CSI	0.06 with VSI and 0.05 with CSI	NA	NA	Not
6	E. Babaei, et. al. [22]	Direct Converter	65	0	7.07 (Average)	NA	NA	Not
7	A. Benhail, et al. [23]	TDVR-PI	30	2.18	24	NA	NA	Not
8	J. Ye, et.al. [26]	Elliptical Restoration	60	NA	NA	NA	0.75	Not
9	R. Omar, et.al [28]	DVR-Super-capacitor	30	0	NA	2.38	NA	Not
10	C.K. Sundara-balan, et. al. [29]	CAESPDVR-ANFIS	46.67 (Average)	0.4	2.35	NA	NA	Not
11	V.K. Awaar, et al. [31]	VSI-SPWM-NI-myRIO-1900-Labview	50	8.79	NA	NA	NA	Yes
12	A.Kiswantono et al. [32]	UVTG-DVR-BES-PV	80	2.89 (Average)	5.81 (Average)	NA	NA	Not
13	**Proposed Study**	**UVTG-DVR-BES-Arduino-Uno-Labview**	**80**	**Bulb=6.4 FL =26.13 LED=8.87**	**NA**	**Bulb=1.523 FL=1.523 LED=1.010**	**Bulb=0.985 FL=0.985 LED=0.990**	**Yes**

Note: NA = note available

is able to produce the source THD_I for bulb lamp, FL lamp, and LED lamp of 17.647%, 11.111%, and 1.010% respectively. Otherwise, for the same system with sag voltage is able to result source THD_I. for bulb lamp, FL lamp, and LED lamp of 1.523%, 1.523%, and 1.010% respectively.

Fig. 13 shows that the system without voltage sag is able to produce the same load THD_I for bulb lamp, FL lamp, and LED lamp of 0.1001%. Otherwise, for

the same system with voltage sag is able to result in load THD_I for bulb lamp, FL lamp, and LED lamp of 0.204%, 0.604%, and 2.564% respectively. Fig. 10 and Fig. 11 shows in the case of voltage sag and three types of loads, the LHE lamp is able to result in the best performance because it is able to produce the highest source true power factor(Pf_{true}) of 0.990 pu and the lowest source THD_I of 1.010%. The source THD_I and load THD_I value in voltage sag also had met the IEEE 519.

Table 6 shows the validation of the results for the proposed study compared to the 12 previous studies. The parameters observed are depth of sag of V_S, sag deviation of V_L, load THD_V, source THD_I, and real-time simulation. At [8], D.N. Katole, et.al proposed an improved SRF on the single-phase DVR series. With a depth of sag of V_S of 42%, this method produces a sag deviation of V_L of 7.6%. Furthermore, the FLC method for sag stress compensation was proposed by M.T. Hagh, et.al [10]. With a depth of sag of V_S of 92% without and 95% with DG, the FLC method yields a sag deviation of V_L of 8.9% without DG and 6.4% with DG, and a load THD_V of 1.26% without DG and 3.54 with DG. The SOGI-PLL method proposed by Yada et. Al [16], with a depth of sag of V_S of 30% was able to produce a sag deviation of V_L of 3.0%. S. Galeshi, et. al [17] already offer Multilevel Cascade H-Bridge Inverter topology. With a depth of sag of V_S of 20%, this topology produces a sag deviation of V_L of 0% and a load of THD_V of 4%. IDVR configuration with VSI and CSI has been proposed by R. Nittala, et.al [19]. With a depth of sag of V_S of 27.7% (with VSI and CSI), this configuration resulted in a sag deviation of V_L of 0%, load THD_V of 0.06% (with VSI) and 0.05% (with CSI). E. Babaei, et. al [22] have proposed a direct converter topology to mitigate voltage sag. With a depth of sag of V_S of 65%, this topology produces a sag deviation of V_L of 0% and a load THD_V of 7.07% (average).

The TDVR-PI configuration has been proposed by A. Benhail, et.al. [23]. With a depth sag of V_S, of 30%, this configuration results in a sag deviation of V_L of 2.18% and a load THD_V of 24%. J. Ye, et.al [26] have proposed an elliptical restoration method for voltage sag compensation and power factor correction. With a depth of sag of V_S, of 60%, this method is able to produce a source pf_{true} of 0.75 pu. The DVR-Super-capacitor configuration has been implemented by R. Omar, et.al [28]. With a depth of sag of V_S, of 30%, this topology is able to produce a sag deviation of V_L of 0 % and source THD_I of 2.38%. The CAESPDVR-ANFIS topology has been investigated by C.K. Sundarabalan, et. al. [29]. With a depth of sag of V_S, of 46.67% (average), this topology was able to produce a sag deviation of V_L of 0.4% and a load of THD_V of 2.35%. V.K. Awaar, et.al. [31] have implemented a VSI-SPWM-based single-phase DVR model with the NI-myRIO-1900 interface monitored in real-time by LabVIEW. With a depth of sag of V_S, of 50%, this model was able to produce a sag deviation of V_L of 8.79%. DVR control supplied by BES-PV using the UVTG method has been observed by A. Kiswantono [32]. With a depth of sag of V_S, of 80%, this configuration and method were able to produce a sag deviation of V_L of 2.89% (average) and a load THD_V of 5.81% (average). Based on the results of research [31] and [32], then this study has implemented the single-phase DVR model using the UVTG method with the Arduino-Uno interface monitored in real-time by LabVIEW. With a depth of sag of V_S of 80%, the proposed model is able to produce sag deviation of V_L of 6.4% (Bulb), 26.13% (FL), and 8.87% (LED). The model is also able to produce THD_I source of 1.523% (Bulb), 1.523% (FL), and 1.101% (LED) and pf_{true} respectively 0.985% (Bulb), 0.985% (FL), and 0.909% (LED). The proposed study is able to give the best performance because it is able to produce source THD_I lower than [28] and source pf_{true} is higher than [26]. Another contribution is that by using the Arduino-Uno interface, the proposed model can be run and monitored in real-time with LabVIEW. It is different from the simulations conducted by 12 previous researchers (except [31]) which were still carried out off-line using Matlab/Simulink environment.

4. Conclusion

The system using a single-phase DVR supplied by BES with load voltage controlled by a UVTG method has been implemented. The model is connected to three types of linear/non-linear load i.e. bulb lamp, FL lamp, and LED lamp. This configuration is proposed to mitigate 80% voltage sag using the Arduino-Uno hardware and monitored by LabVIEW simulation in real-time. The investigated parameter is source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power-factor measurements are also carried out to obtain the harmonics of the source current and load current. During voltage sag, the single-phase DVR-BES system is able to maintain load voltage for all types of loads. From the system with voltage sag and three different types of loads, the LHE lamp is able to result in the best performance because it is able to produce the highest source current power factor (pf_{true}) and

the lowest source THD_I. The source THD_I and load (THD_I) with voltage sag also had met the IEEE 519. The proposed study is able to give the best performance because it is able to produce source THD_I lower than the previous studies. By using the Arduino-Uno interface, this model can be run and monitored in real-time with LabVIEW better from the simulations conducted by previous researchers which were still carried out off-line using Matlab/Simulink.

In a system using a single-phase DVR-BES connected to the FL load, there is a significant increase in load voltage of 256 V compared to the source voltage. The percentage of sag voltage for FL lamps also increased by 26.13% and has far exceeded the value of 5%. The implementation of a single-phase bidirectional inverter circuit as the interface between the BES and series active filters can be proposed as future work to overcome this problem. The measurement of source THD_V and load THD_V in the proposed model is also necessary to determine the harmonic mitigation performance of the voltage within the IEEE 519 limit.

Conflicts of Interest

The authors declare no conflict of interest.

Author Contributions

Conceptualization, Y.A. Setiawan and A. Amirullah; methodology, Y.A. Setiawan and A. Amirullah; software, Y.A. Setiawan; validation, Y.A. Setiawan; formal analysis, Y.A. Setiawan and A. Amirullah; investigation, Y.A. Setiawan and A. Amirullah; resources, Y.A. Setiawan; data curation, Y.A. Setiawan; writing—original draft preparation, Y.A. Setiawan; writing—review and editing, Y.A. Setiawan; visualization, Y.A. Setiawan; supervision, A. Amirullah; project administration, Y.A. Setiawan; funding acquisition, A.Amirullah. All authors read and approved the final manuscript.

Acknowledgments

The authors would like to acknowledge to Institutions of Research and Community Service Universitas Bhayangkara Surabaya, for funding to this research base on Decree Letter Number 65/XI/2020/UBHARA date 19 November 2020.

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Lampiran 2.10

Bukti Official Receipt

Pembayaran Makalah

Intelligent Networks and Systems Society

Official Receipt

International Journal of Intelligent Engineering and Systems (IJIES)

January 22 2021

Received from

Amirullah Amirullah
Universitas Bhayangkara Surabaya

Description	Unit	Amount
IJIES formatting fee	1	USD 350
Total		USD 350

Prof. Dr. Kei EGUCHI
President, International Journal of Intelligent Engineering and Systems

Department of Information Electronics
Fukuoka Institute of Technology

Kei Eguchi

E-mail: ijies@inass.org

Lampiran 2.11

Bukti Acceptance Letter

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Acceptance Letter

International Journal of Intelligent Engineering and Systems (IJIES)

January 22, 2021

Dear Amirullah Amirullah,

Manuscript Title: Implementation of Single-Phase DVR-BES Based on Unit Vector Template Generation (UVTG) to Mitigate Voltage Sag Using Arduino Uno and Monitored in Real-Time Through LabVIEW Simulation

Author(s): Yohanes Artha Setiawan, Amirullah Amirullah

Thank you for submitting your paper to the International Journal of Intelligent Engineering and Systems (IJIES). Based on double blind review process, we are pleased to inform you that our Review Committee has accepted your paper.

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We are looking forward to your further contribution to our journal.

Kind regards

Prof. Dr. Kei EGUCHI
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