2-3 March 2010

ISSN: 2086-4868

ICGC-RCICT 2010

PROCEEDINGS OF

THE FIRST INTERNATIONAL CONFERENCE ON GREEN COMPUTING

AND

THE SECOND AUN/SEED-NET REGIONAL CONFERENCE ON ICT

DEPARTMENT OF ELECTRICAL ENGINEERING
AND INFORMATION TECHNOLOGY
FACULTY OF ENGINEERING
GADJAH MADA UNIVERSITY

Department of Electrical Engineering
and Information Technology
Faculty of Engineering
Gadjah Mada University
Jalan Grafika no 2 Kampus UGM
Yogyakarta, 55281, Indonesia

Proceedings of The First International Conference on Green Computing and The Second AUN/SEED-Net Regional Conference on ICT

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Yogyakarta, 2 – 3 March 2010

DEPARTMENT OF
ELECTRICAL ENGINEERING AND INFORMATION TECHNOLOGY
FACULTY OF ENGINEERING
GADJAH MADA UNIVERSITY

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Foreword

With the number of human population is getting higher and higher, the ability of our environment to support human life is gaining its importance. Sustainable development, or development that meets the needs of the present without sacrificing the future, has since then been adopted by many countries and institutions at all levels.

In supporting sustainable development, the field of information and communication technology (ICT) has coined the term “green ICT” or “green computing”, which describes the study and practice to use computing resources efficiently. As a contemporary issue, green computing becomes an important concern for big industries, small companies, and even government institutions since their success criteria are no longer based on a single measure.

Unfortunately, green computing has not been widely understood, yet practiced effectively. Not many technological options have been explored, and still it is mainly viewed from technological and engineering perspectives only. The challenges are thus twofold: exploring technological advances to achieve better ICT utilization, and how technology products/solutions can be applied effectively to meet the specified success criteria. These challenges are even more relevant to developing countries, since they are less exposed to scientific frontiers and have shorter tradition and less experiences of ICT utilization. On the other hand, these countries bear heavier burdens due to digital divide phenomenon which may block the road to the fulfillment of Millenium Development Goals in 2015. Therefore it is considered important to pave roads towards green computing, especially its application in developing countries. Many aspects have to be explored, considered, and discussed in an interdisciplinary manner, and this becomes the purpose of this conference.

The First International Conference on Green Computing (ICGC 2010) is an event organized by the Department of Electrical Engineering and Information Technology, Faculty of Engineering, Gadjah Mada University. This year, ICGC 2010 is held in conjunction with the AUN/SEED-Net’s Regional Conference on ICT 2010 (RC-ICT 2010). AUN/SEED-Net is a network of engineering education higher institutions in ASEAN countries. The event also commemorates the 64 years of Faculty of Engineering, Gadjah Mada University, as well as celebrates the inauguration of the new name of Department of Electrical Engineering and Information Technology.

It is expected that ICGC 2010 and RC-ICT 2010 can serve as a forum for sharing knowledge and experiences in the ICT field under the ASEAN spirit. Hosting 82 papers from Thailand, Vietnam, Laos, Cambodia, Myanmar, Malaysia, Philippines, India, Japan, and Indonesia, including speakers from government and industry, the conference is expected to yield fruitful outcomes for the benefit of all participating researchers, institutions, and countries.

Finally, as the Chairman of the Organizing Committee, I would like to express my deep appreciation to ASEAN Foundation, JICA, AUN/SEED-Net, King Mongkut’s Institute of Technology Ladkrabang, for invaluable support and assistance. My big thanks also go to all members of the Organizing Committee who have devoted their time and energy for the success of the event.

For all participants, I wish you an enjoyable conference in this colourful city of Yogyakarta.

Dr. Lukito Edi Nugroho
Chairman of the Organizing Committee

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[Note: Yogyakarta time leads the UCT (Formerly GMT) by seven hours]

Conference Day ONE: Tuesday, 2 March 2010

08.00 – 08.30: Registration

08.30 – 09.15: Opening Ceremony

1. Chairman of the Organizing Committee
2. Rector of UGM
3. ASEAN Foundation Executive Director
4. AUN/SEED-Net Executive Director

09.15 – 09.30 Photo Session

09.30 – 10.00 Morning Coffee Break

PLENARY SESSION: SPECIAL LECTURE (at Room A)

Moderator: Sarjiya

10.00 – 10.30 Ministry of Communication and Informatics, Republic of Indonesia…

10.30 – 11.00 **Mr. Aris Dinamika**
PT Schneider Indonesia
Energy Efficiency: A Mandatory Driver for a Changing World

11.00 – 11.30 **Prof. Singo Yoshizawa**
Graduate School of Information and Science Technology, Hokkaido University, Sapporo, Japan
Experimental Platform in 5-GHz Band Wireless Communication Using an 80-MHz Bandwidth MIMO-OFDM System

11.30 – 12.00 **Prof. Shinji Hara**
Department of Information Physics and Computing, The University of Tokyo, Japan
Hierarchical Consensus for Large Scale Networked Dynamical Systems

12.00 – 13.15 Lunch

13.15 – 16.10 **PARALLEL SESSION (Room A, B, C, D):** Listed in the following pages

18.30 **Conference Dinner**

Conference Day TWO: Wednesday, 3 March 2010

PLENARY SESSION: SPECIAL LECTURE (at Room A)

Moderator: Suharyanto

08.30 – 09.00: **Prof. Kazuhiko HAMAMOTO**
Dept. of Information Media Technology, School of Information and Telecommunication Eng., Tokai University, Tokyo, Japan
Virtual Reality and Augmented Reality and their Applications to Medical Diagnosis and Green Computing

09.00 – 09.30: **Prof. Yoshiteru Ishida**
Department of Knowledge-Based Information Engineering, Toyohashi University of Technology, Aichi, Japan
Ubiquitous Sensor Networks for Monitoring the Environment: Adaptive Sensing Based on Profiles

09.30 – 10.00 **Prof. Hiroshi Shigeno**
Graduate School of Science and Technology, Keio University, Kanagawa, Japan
Filter Multicast: A Communication Support for Dynamic Vehicle Platoon Management

10.00 – 10.30 **Morning Coffee Break**

10.30 – 15.40 **PARALLEL SESSION (at Room A, B, C, D):** listed in the following pages

12.10 – 13.10 **Lunch**

13.10 – 15.10 **PARALLEL SESSION** (cont.)

15.10 – 15.30 **Afternoon Coffee Break**

15.30 – 17.00 **AUN/SEED-Net Members:** Discussion (Room A)

PARALLEL SESSION (Room A, B, C, D)

Allocated duration per paper : 20 minutes (max.)
- GREEN lamp : 10 minutes (max.) presentation
- YELLOW lamp : 10 minutes (max.) discussion
- RED lamp : END of allocated duration

Conference Day ONE: Tuesday, 2 March 2010

Room: A
Committee on duty: Bagas Nawolo Seto

Time	Code	(First) Author	Paper Title
		Moderator A11: Annanda Thavymony RATH **Co-Moderator :** F. Danang Wijaya (Committee)	
13.15-13.35	*IND #1*	*P.U. Bhalchandra*	*Epitomizing Green Computing*
13.35-15.55	JPN #1	Thida Zin Myint	Range-Free Localization Algorithm Using Distance Deviation …
15.55-14.15	JPN #2	Sach Thanh LE	Stereo-Based Ground Plane Estimation: A Reliable Approach for …
14.15-14.35	CAM #1	Chanthea Khun	Analysis of Single-Phase Passive and Active EMI Filter Performance …
14.35-14.55	CAM #2	Vuthchhay Eng	Dynamic Modeling and Control of a SEPIC Converter in …
14.55-15.10		**Afternoon Coffee Break**	
		Moderator A12: Chanthea Khun / Vuthchhay Eng **Co-Moderator :** Husni Rois Ali (Committee)	
15.10-15.30	CAM #3	A.T. RATH	Prototype of Sound-based News on Demand Application in…
15.30-15.50	MYA #1	Khin Mar Soe	Sustainable Development of ICT for Rural Areas in Myanmar
15.50-16.10	MYA #2	Soe Soe Khaing	Green in ICT Utilization for Sustainable Development of Myanmar

Room: B
Committee on duty: Arief Hartawan Putro

Time	Code	(First) Author	Paper Title
		Moderator B11: S. W. Harun/ Kamal Z. Zamli **Co-Moderator :** Enas Dhuhri Kusuma (Committee)	
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13.35-15.55	SIN #1	Nhan H. Truong	Fair End-to-end Bandwidth Allocation (FEBA) Algorithms …
15.55-14.15	SIN #2	Binh P. Nguyen	Cross Directional Rectangle Search for Fast Block-Matching Motion …
14.15-14.35	SIN #3	Trang T.T. Do	A High-Accuracy and High-Speed 2-D 8x8 Discrete Cosine …
14.35-14.55	MAS #1	F.R. M. Adikan	Flat Fibre technology: towards a truly flexible, distributed optical …
14.55-15.10		**Afternoon Coffee Break**	
		Moderator B12: F.R. Mahamd Adikan **Co-Moderator :** Igi Ardiyanto(Committee)	
15.10-15.30	MAS #2	S. W. Harun	Compact Bismuth-based Erbium-doped Fiber Amplifier With …
15.30-15.50	MAS #3	Kamal Z. Zamli	Adopting Variable Strength Interaction Testing: Some Practical Issues
15.50-16.10	*MAS #4*	Moh. A. Ramlan	Optimum Operation of Pump at Water Treatment Plant for Achieving ….

Room: C
Committee on duty: Fajar Subekti Wirawan

Time	Code	(First) Author	Paper Title
		Moderator C11: Khoi Phan-Dinh /Son Hong Ngo/ Tran Ngoc Thinh **Co-Moderator :** Lesnanto (Committee)	
13.15-13.35	INA #1	Achmad Imam K.	Experiences in Implementing General-Purpose Applications on CUDA
13.35-15.55	PHI #1	Rose Ann Sale	KineSpell2 A Full VAK Approach in Learning Spelling
15.55-14.15	PHI #2	Cesar A. Llorente	Event Driven Reconfigurable Architecture for Real-time Multiple …
14.15-14.35	VIE #1	Nguyen T.T.Tu	A Proposal of Internet-based Monitoring and Control Systems Using ….
14.35-14.55	VIE #2	Phong Tuan Ngo	Providing Qualified Intensional Answers Using Fuzzy Concept Hierarchies
14.55-15.10		**Afternoon Coffee Break**	
		Moderator C12: Nguyen Thi Thanh/Tu Phong Tuan Ngo **Co-Moderator :** Ridi Ferdiana (Committee)	
15.10-15.30	VIE #3	Son Hong Ngo	Credibility checking-based scheduling schemes for desktop grid …
15.30-15.50	VIE #4	Khoi Phan-Dinh	New Method to Implement Intelligent Street Lighting System in Vietnam
15.50-16.10	VIE #5	Tran Ngoc Thinh	High-throughput Pattern Matching Engine for Network Intrusion …

Certificate of presentation is available after completing your presentation.

Room: D, day ONE
Committee on duty: Azhar Sukma Alam

Time	Code	(First) Author	Paper Title
		Moderator D11: Sopon Pumeechanya /Pornchai Korpraserttaworn/ Keokanlaya Sihalath **Co-Moderator :** Avrin Nur Widyastuti (Committee)	
13.15-13.35	LAO #1	Khamphong K.	3D Reconstruction from X-ray Fluoroscopy using Exponential …
13.35-15.55	THA #1	Simon J. Q. Lam	Error Concealment in H.264 Spatial Scalable Video using Improved …
15.55-14.15	THA #2	D. LAKANCHANH	Evaluation of Blind Modulation Detection in Adaptive OFDM Systems
14.15-14.35	THA #3	Nayot K.	An Algorithm for Q-Factor Evaluation A Case Study on 40 Gbps …
14.35-14.55	THA #4	Napat R.	On-line Verification Algorithm for Flexible Interval Representation …
14.55-15.10		**Afternoon Coffee Break**	
		Moderator D12: Simon J. Q. Lam/ D. LAKANCHANH/ Napat R. **Co-Moderator :** Eny Sukani Rahayu (Committee)	
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15.30-15.50	THA #6	Pornchai K.	Running Network Intrusion Detection System on a Recycled Personal …
15.50-16.10	THA #7	K. Sihalath	Directional Filtered Fingerprint Images: An Investigation and …

PARALLEL SESSION (Room A, B, C, D)
Conference Day TWO: Wednesday, 3 March 2010

Room: A
Committee on duty: Ahmad Muqurobin H.T. Moderator Assistant: Iqbal Mustika

Time	Code	(First) Author	Paper Title
		Moderator A21: Handaru Jati	
10.30-10.50	Pale #2	Rendra G.	An Integrated Model of Collaborative Learning in Higher Education
10.50-11.10	Sura #1	A. S. Rachman	Energy-Efficient Protocol of Wireless Sensor Network using …
11.10-11.30	Sura #2	S. Tahcfulloh	Performance Evaluation of Adaptive Coded Modulation and …
11.30-11.50	UNY #1	Ratna Wardani	Providing User Quality of Service Specification for Communities with …
11.50-12.10	Sura #3	Gunawan	Efficiency Comparison on Eclat, FP-Tree, and Top-Down Algorithms …
12.10-13.10		**Lunch**	
		Moderator A22: Ratna Wardani	
13.10-13.30	Sura #4	Gunawan	Collocation Detection for Indonesian
13.30-13.50	Sema #2	Ida Widihastuti	Image Processing Intelligent System Iris Eye Real-Time Compound …
13.50-14.10	UNY #3	Handaru Jati	Analysis of Green Computing Strategy in University: Analytic …
14.10-14.30	UNY #4	Handaru Jati	Website Quality Evaluation Comparison: An Empirical Study in Asia
14.30-14.50	AAU #1	Arwin Datumaya	Knowledge Sharing in Knowledge-Growing-based Systems
14.50-15.10	AAU #2	Rakhmat Hidayat	Savings Time Execution Prima Numbers Generator Using Bit-Array …
15.10-15.30		**Afternoon Coffee Break**	

Certificate of presentation is available after completing your presentation.

Room: B, day TWO
Committee on duty: Arief Herusetyo Wicaksono Moderator Assistant: Tiko Raharianto

Time	Code	(First) Author	Paper Title
		Moderator A21: Fatchul Arifin	
10.30-10.50	Bali #1	I K G Darma P.	SMS Based Technology For Data School Collecting In Bali
10.50-11.10	Madu #1	Rima Tri W.	Smile Stages Recognition in Orthodontic Rehabilitation Using …
11.10-11.30	Sura #5	Patria Julianto	Optimization of Size and Location of Capacitor Banks on Distribution …
11.30-11.50	Sura #6	Thiang	Position Control of Manipulator's Links Using Artificial Neural …
11.50-12.10	TETI #12	Udayanto Dwi A.	Design of Power Plant Boiler Temperature Monitoring Application …
12.10-13.10		**Lunch**	
		Moderator A22: Udayanto Dwi Atmojo	
13.10-13.30	UNY #2	Fatchul Arifin	ElectroLarynx, Esopahgus, and Normal Speech Classification using …
13.30-13.50	Sala #1	Irwan Sembiring	Data Authentication in Network Forensic Using MD5 and CRC32 Method
13.50-14.10	TETI #21	Herdjunanto S.	Green Analysis : a System Approach A Case Study: Sensor Fault …
14.10-14.30	TETI #22	Herdjunanto S.	Computation Time Reduction as a Strategy to Reduce Energy in …
14.30-14.50	TETI #31	Wahyuni	Information Technology Infrastructure Flexibility and …
14.50-15.10	TETI #32	Avrin N. W.	Analysis of Solar Cell Traffic Light System in Kota Yogyakarta
15.10-15.30		**Afternoon Coffee Break**	

Room: C, day TWO

Committee on duty: Ircham Ardani, Moderator Assistant: Andreas W. Octavian

Time	Code	(First) Author	Paper Title
		Moderator A21: Vita Lystianingrum	
10.30-10.50	Jaka #1	Hadian S. Utama	Design and Implementation of Solar Tracker in Solar Energy …
10.50-11.10	Jaka #2	Yulianus	The Assesment of Quality of Service (QoS) in IP/MPLS Network
11.10-11.30	Sura #8	Andy Noortjahja	Filtering of normal, and laryngectomiced patient voices using …
11.30-11.50	Sura #9	Ingrid Nurtanio	Compression and Reconstruction of Digital Dental Image on Fuzzy …
11.50-12.10	Maka #1	Mingsep S.	The Internet Protocol Design Framework To Real Time …
12.10-13.10		**Lunch**	
		Moderator A22: Mingsep Sampebua	
13.10-13.30	Sura #7	Vita L.	Maximum Power Point Tracker Using Buck-Boost Converter as …
13.30-13.50	Sema #1	Sari Wijayanti	Application of Decision Support System to Determine the Level of …
13.50-14.10	TETI #26	P. Insap Santosa	Gesture-based Mouse Cursor Movement Using Template-Matching: …
14.10-14.30	TETI #27	Widyawan	Low-Powered Wireless Sensor Network for Indoor Localization
14.30-14.50	TETI #28	Enas Dhuhri K.	Developing Multi-applicationed smart card system with ITSO standard
14.50-15.10	TETI #29	Enas Dhuhri K.	Image Processing Using ARM9-based Embedded System Case Study: ..
15.10-15.30		**Afternoon Coffee Break**	

Room: D, day TWO

Committee on duty: Fajar Budi Suryawan Moderator Assistant: Teguh Afandi

Time	Code	(First) Author	Paper Title
		Moderator: Budhy Setiawan	
10.30-10.50	Pale #1	Deris Stiawan	Reliability Measurement of Internet Services
10.50-11.10	Sura #10	Lilik Anifah	Simulation of Desicion Support System for Pricing Grid Enterprise in …
11.10-11.30	Sura #12	Mardlijah	Design and Performance Analysis of Speed Controller in Induction …
11.30-11.50	Sura #13	Saidah	High Performance of Nonlinear DC Motor Speed Control using ...
11.50-12.10	Papu #1	Maurits A. Paath	The Evaluation of Non-fundamental Frequency Apparent Power and …
12.10-13.10		**Lunch**	
		Moderator: Maurits A. Paath	
13.10-13.30	Sura #11	Budhy Setiawan	Backpropagation Neural Network based Reference Control Modeling …
13.30-13.50	TETI #11	Sri Arttini D.P.	Adaptive LMS Noise Cancellation of Wideband Vehicle's Noise Signals
13.50-14.10	TETI #24	M. Isnaeni B.S.	PLC-based Power Factor Regulator
14.10-14.30	TETI #23	Risanuri Hidayat	Embedded Webserver Applications for Industrial Process Monitoring
14.30-14.50	TETI #25	Astria N Irfansyah	Implementation of Low Cost Modbus Protocol-Enabled Embedded …
14.50-15.10	TETI #30	Budi Setiyanto	QAM Mapper-Demapper for an Adaptive Modulation OFDM: from …
15.10-15.30		**Afternoon Coffee Break**	

Certificate of presentation is available after completing your presentation.

High Performance of Nonlinear DC Motor Speed Control using Backpropagation Neural Network

Saidah[1,2], Mohamad Ashari[1] , Mauridhi Heri purnomo[1]

[1]Departement of Electrical Engineering, Institute Technology Sepuluh Nopember, Surabaya Indonesia
[2]Departement of Technology Engeneering, Bhayangkara University, Surabaya, Indonesia

Abstract— Conventional PID of controllers for nonlinier DC motors have poor performance when changes of the motor or load dynamics take place. To make improve the performance, an adaptive neural speed controller of a nonlinier dc motor is proposed. BackPropagation neural network (BPNN) is used to appoximate the unknown dynamics. BPNN is trained by the online backpropagation algorithm. The output of the BPNN gives the control voltage applied to the dc motor. The difference between the reference and the actual rotor speed of the nonlinier motor is backpropagated through the BPNN at each step of the control process for updating the connection weights of the BPNN. The control scheme requires neither a knowledge of any motor parameters, nor preferential training of the BPNN. The performance of the controller is simulated and then it is compared with conventional controller or PID in fluctuation disturbance.

Keywords-component; Nonlinier DC Motor; BPNN;

I. INTRODUCTION

DC motors are widely used in industrial systems, such as robotic manipulators, because their control is relatively simple and they are reliable for a wide range of operating conditions. DC motors are usually modelled as linear systems and then linear control approaches are implemented. However, most linear controllers have unsatisfactory performance due to changes of the motor/load dynamics and due to nonlinearities introduced by the armature reaction. Neglecting the impact of external disturbances and of nonlinearities may risk the stability of the closed-loop system. For the aforementioned reasons DC motor control based on conventional PID or model based feedback controllers can be inadequate and more effective control approaches are needed. If the nonlinearities of the motor are known functions, then adaptive tracking control methods with the technique of input–output linearization can be used [1,2]. However, when these nonlinearities or disturbances are unknown, neural or fuzzy control is more suitable for succeeding satisfactory performance of the closed-loop system [3–7]. Results on the successful application of neural identification and control to dc motor drives have been given in [8–10], were neural network controllers for a dc motor were introduced. the unknown nonlinear dynamics of the motor and the external load torque were approximated by a multi-layer neural network.

This paper proposes a method for the control of DC motors, To make high performance an adaptive neural speed controller of a nonlinier dc motor is proposed. The Back Propagation neural network (BPNN) is used to appoximate the unknown dynamics. BPNN is trained by the online backpropagation algorithm. The output of the BPNN gives the control voltage applied to the dc motor. The difference between the reference and the actual rotor speed of the nonlinier motor is back propagated through the BPNN at each step of the control process for updating the connection weights of the BPNN. The control scheme requires neither a knowledge of any motor parameters, nor preferential training of the BPNN. The performance of the controller is simulated and then it is compared with conventional control or PID in fluctuation disturbance.

II. THE DC MOTOR MODEL

A direct current (DC) motor model converts electrical energy into mechanical energy. There are two main ways in controlling a DC motor: the first one named *armature control* consists of maintaining the stator magnetic flux constant, and varying (use as control input) the armature current. Its main advantage is a good torque at high speeds and its disadvantage is high energy losses. The second way is called *field control*, and has a constant voltage to set up the armature current, while a variable voltage applied to the stator induces a variable magnetic flux. Its advantages are energy efficiency, inexpensive controllers and its disadvantages are a torque that decreases at high speeds [11]. A linear model that approximates the dynamics of the DC motor is derived as follows: the torque developed by the motor is proportional to the stator's flux and to the armature's current thus one has

$$\Gamma = k_f \psi K_\alpha I \quad (1)$$

Where Γ is the shaft torque, ψ is the magnetic flux in the stator field, I is the current in the motor armature. Since the flux is maintained constant the torque of Eq. (1) can be written as

$$\Gamma = k_T I \ , \quad \text{where} \quad k_T = k_f \Psi K_\alpha \quad (2)$$

A part from this, when a current carrying conductor passes through a magnetic field, a voltage V_b appears corresponding to what is called electromagnetic force (EMF)

$V_b = K_e\omega$ (3)

Where ω is the rotation speed of the motor shaft. The constants k_T and k_e have the same value. Kirchoff's law yields the equation of the motor (Fig. 1) :

$V - V_{res} - V_{coi} - V_b = 0$ (4)

Where V is the input voltage, V_{res} = RI is the armature resistor voltage (R denotes the armature resistor), V_{coil} = LI is the armature inductance voltage. The motor's electric equation is then

$$L\dot{I} = -k_e\omega - RI + V \quad (5)$$

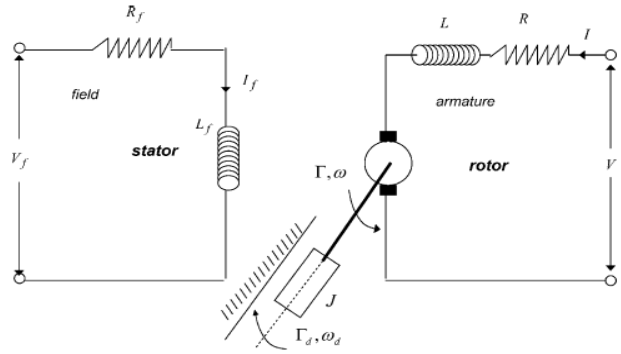

Fig. 1. Parameters of the DC motor model.

From the mechanics of rotation it holds that

$$J\dot{\omega} = k_e I - k_d\omega - \Gamma_d \quad (6)$$

The DC motor model is finally

$$\begin{aligned} L\dot{I} &= -k_e\omega - RI + V \\ J\dot{\omega} &= k_e I - k_d\omega - \Gamma_d \end{aligned} \quad (7)$$

With the following notations

Notation	Significance
L	armature inductance
I	armature current
k_e	motor electrical constant
R	armature resistance
V	input voltage, taken as control input
J	Motor inertia
ω	rotor rotation speed
k_d	mechanical dumping constant
Γ_d	disturbance torque

Where the armature designates the iron cored rotor wound with wired coils. Assuming $\Gamma_d = 0$ and denoting the state vector as $(\mathbf{x}_1, \mathbf{x}_2, \mathbf{x}_3)^{\mathbf{T}} = (\boldsymbol{\theta}, \dot{\boldsymbol{\theta}}, \ddot{\boldsymbol{\theta}})^{\mathbf{T}}$ a linier model of the DC motor is obtained :

$$\begin{pmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{pmatrix} = \begin{pmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & \frac{-k_e^2 - k_d R}{JL} & \frac{-JR - k_d L}{JL} \end{pmatrix} \begin{pmatrix} x_1 \\ x_2 \\ x_3 \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \\ \frac{k_e}{JL} \end{pmatrix} V \quad (8)$$

Usually the DC motor model is considered to be linear by neglecting the effect of armature reaction or by assuming that the compensating windings remove this effect. Introducing the armature reaction leads to a nonlinier system and in that case a nonlinier model may be appropiate. In that case the dynamic model of the DC motor model can be written as [5]:

$$\dot{x} = f(x) + g(x)u \quad (9)$$

With denoting the derivative of the motor's state vector, $\mathbf{X} = [\mathbf{x}_1, \mathbf{x}_2, \mathbf{x}_3]^{\mathbf{T}} = [\boldsymbol{\theta}, \dot{\boldsymbol{\theta}}, \mathbf{i}_a]^{\mathbf{T}}$. The functions f(x) and g(x) are vector field functions defined as :

$$f(x) = \begin{pmatrix} x_2 \\ k_1 x_2 + k_2 x_3 + k_3 x_2^2 + k_4 T_1 \\ k_5 x_2 + k_6 x_2 x_3 + k_7 x_3 \end{pmatrix}, \quad g(x) = \begin{pmatrix} 0 \\ 0 \\ k_8 \end{pmatrix} \quad (10)$$

Where $k_1 = -F/J$, $k_2 = A/J$, $k_3 = B/J$, $k_4 = -1$

$k_5 = -A/L$, $k_6 = -B/L$, $k_7 = -R/L$, $k_8 = -1/L$

A block diagram of nonlinier DC motor is shown in Fig. 2. with speed variable as output.

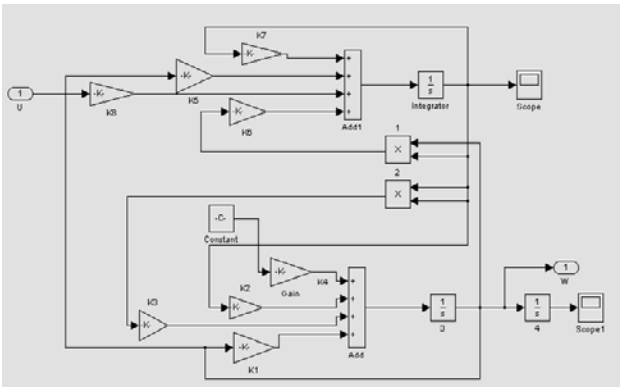

Fig 2. Block scheme of Nonlinier DC Motor

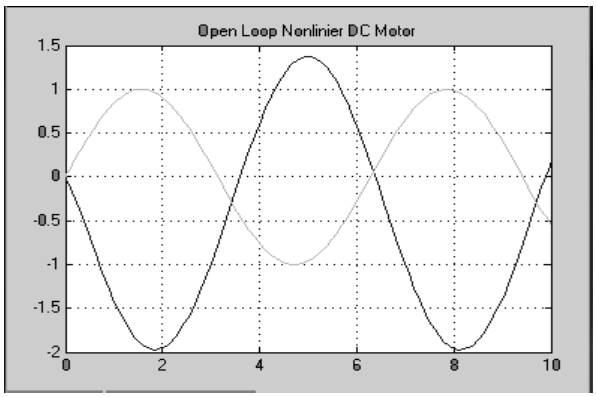

Fig. 3. Effect of nonlinear in open-loop control mode

Fig. 3 shows the effect of these nonlinearities on DC motor system. The speed response of the system to a sinusoidal control voltage is measured in open loop using a tachometer mounted on the load side.

III. BPNN THOPOLOGY

A general structure of a multi-layer NN is shown in Figure 1 [I2]. Such a neural network contains *three* layers: input layer, hidden layer(s) and output layer. Each layer is composed of several neurons. The number of the neurons in the input and output layers depends on the number of the selected input and output variables.

The number of hidden layers and the number of neurons in each depend on the *system* dynamics and the desired degree of accuracy. Usually one layer is adequate in many applications. A trial and error method *can* be used to select a proper number of the hidden neurons.

All the neurons in adjacent layers are interumnected. The strength of the interconnection is determined by the weighting vector of the BPNN.

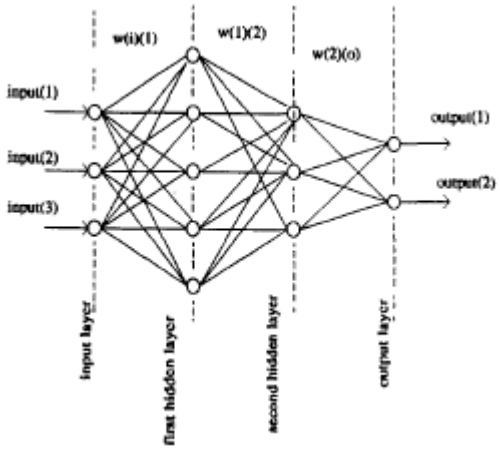

Fig. 4: Multi Layer Neural Network

Each neuron perfinms two functions, as shown in Figure 2. The fust is to sum all the inputs from the upper layer based on their weighting factors as given in equation (11). The second is to process this *sum* by a nonlinear sigmoidal function [I2] as shown in equation (12). The input and output neurons may not contain nonlinear functions.

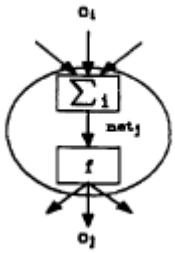

Fig. 5: A Single Neuron

The basic equations describing the dynamics of each neuron are

$netj = \Sigma_i W_{ij}.O_i$ (11)

$0, = f(netj + ej)$ (12)

where:

W_{ij} weight between the j^{th} neuron and the i^{th} neuron in two adjacent layers;

θ_j threshold of the j^{th} neuron;

O_i output of i^{th} neuron;

O_J output of j^{th} neuron;

f (.) sigmoidal function

The BPNN **has** two phases of operation: training and testing. In the training phase, the weights of the BPNN are adjusted to map the input of the system to its output. In the testing phase, the BPNN should predict the correct system output for a given input, even if the input was not used in training.

Fig. 6. Indicate block diagram of nonlinier DC motor using PID controller. The proportional integral derivative (PID) gains of the closed-loop system are adjusted after obtaining by the Ziegler Nichols method [14]. Fig. 7 Indicate block diagram nonlinier DC motor using BPNN controller .

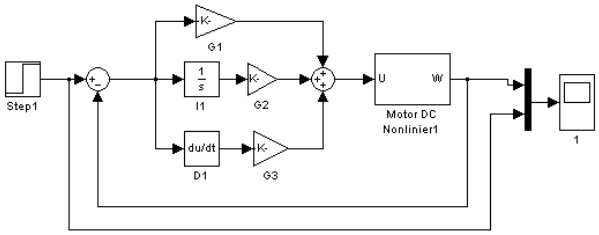

Fig. 6. Block Scheme of nonlinier DC motor with PID controller

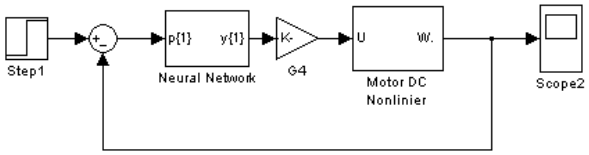

Fig 7. Proposed DC Motor with BPNN controller

IV. SIMULATION RESULT

In this section, we illustrate the efectiveness of the proposed control scheme by computer simulations Figure 8 shows training results of the BPNN controller at the speed control.

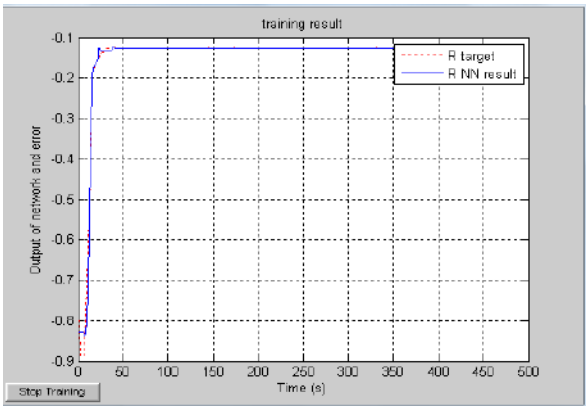

Fig 8. Result training for DC motor speed

The simulation results of the speed control with the step reference signal by the PID controller and by the BPNN controller is in Fig. 9 and Fig. 10. Fig. 11 showed simulation result of the speed control with disturbance by the PID controller and by BPNN.

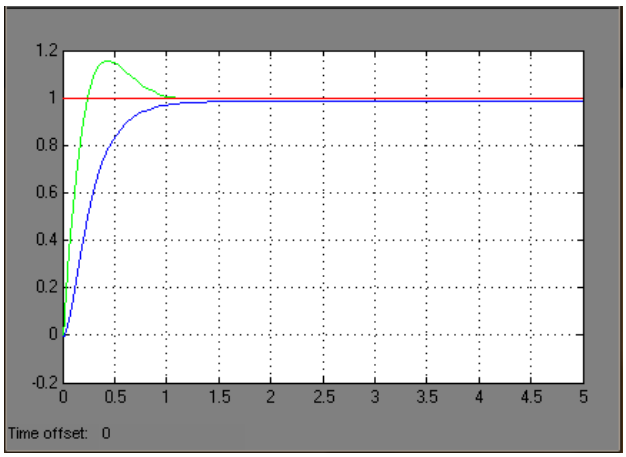

Fig. 9. Simulation results of the speed control with the unit step reference signal (a) by the PID controller and (b) by the BPNN

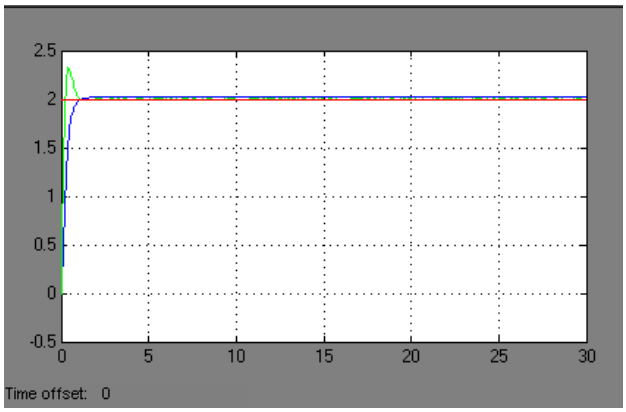

Fig. 10. Simulation results of the speed control with step reference signal (a) by the PID controller and (b) by the BPNN.

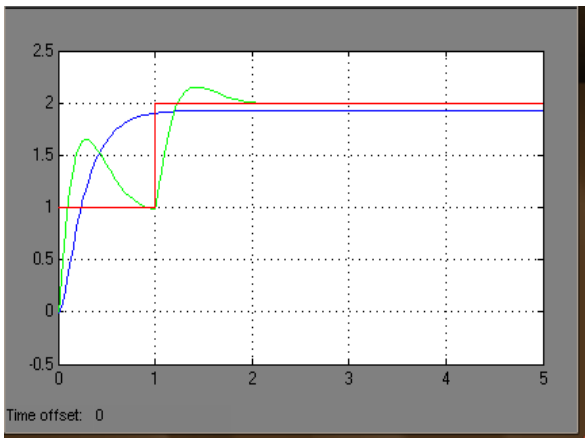

Fig. 11. Simulation results of the speed control with disturbance (a) by the PID controller and (b) by the BPNN

V. CONCLUSION

In this paper, a model-following adaptive control method is developed for the speed control of a nonlinear DC motor system using Back Propagation neural networks (BPNN). In comparison of simulation results with the PI controller, the proposed BPNN controller system can yield a better dynamic performance with shorter settling time and without overshoot. In comparison of simulation results with give disturbance has showen that system can yield a better dynamic performance than PID controller.

ACKNOWLEDGEMENTS

The authors would like to thank the reviewers for their helpful comments.

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CERTIFICATE

This is to certify that

Saidah

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has participated in **The First International Conference on Green Computing** and **The Second AUN/SEED-NET Regional Conference on ICT**, held on 2 - 3 March 2010, at Department of Electrical Engineering and Information Technology, Faculty of Engineering, Gadjah Mada University, as

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