YAYASAN BRATA BHAKTI DAERAH JAWA TIMUR
UNIVERSITAS BHAYANGKARA SURABAYA
LEMBAGA PENELITIAN DAN PENGABDIAN PADA MASYARAKAT
(LPPM)
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SURAT KETERANGAN

Nomor: Sket/ 42 /I/2023/LPPM/UBHARA

Kepala Lembaga Penelitian dan Pengabdian kepada Masyarakat (LPPM) Universitas Bhayangkara Surabaya menerangkan bahwa:

Nama	: Dr. Amirullah, ST, MT.
NIP	: 197705202005011001
NIDN	: 0020057701
Unit Kerja	: Universitas Bhayangkara Surabaya

Benar telah melakukan kegiatan:

1. Mereview makalah jurnal internasional bereputasi berjudul EVALUATION OF CHB MLI BASED SHUNT APF USING LOW PASS FILTER AND SELF-TUNING FILTER dari Journal of Engineering Science and Technology (JESTEC), Publisher: Taylor's University Malaysia Tahun 2022, Terindeks Scopus Q3.
2. Telah melakukan korespondensi email dengan editor/pengelola jurnal dalam rangka mereview substansi materi makalah jurnal dalam selang waktu yang telah ditentukan sebelumnya. Bukti korespondensi email dan bukti pendukung adalah benar sudah dilakukan oleh yang bersangkutan serta sudah dilampirkan bersama surat ini.

Demikian surat keterangan ini dibuat untuk kepentingan kelengkapan pengusulan Guru Besar.

Surabaya, 20 Januari 2023
Kepala LPPM

Drs. Heru Irianto, M.Si.
NIP. 9000028

Lampiran 1

Bukti Korespondensi Email dengan Editor/Pengelola Jurnal

Ubhara Surabaya

Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Paper ID ee2250 /Requesting paper review for JESTEC, First round of Review Process/

6 pesan

Jestec <Jestec@taylors.edu.my> 7 November 2022 pukul 12.39

Dear Dr.

Greetings from the Editorial Board of JESTEC.

The following attached manuscript titled

EVALUATION OF CHB MLI BASED SHUNT APF USING LOW PASS FILTER AND SELF-TUNING FILTER

has been submitted to JESTEC for consideration for publication.

As an expert in its topic area, I am writing to request that you review it and make a recommendation regarding its acceptability..

I hope that you will agree to review this manuscript. I would appreciate, if possible, receiving your review by November 25, 2022.

If you would like to have more time to complete the review, could you please indicate the time frame you expect to return the review report?

I appreciate your contribution in maintaining the quality and value of JESTEC and look forward to your response.

Best regards

Some quick guidelines to our respected reviewers

Whenever appropriate, we would appreciate if you evaluate the paper based on the following seven criteria. Please try not to focus on the editorial issues/mistakes as too many of them may lead to the author's frustration. When we revise their paper, we want the authors to focus on our comments/concern related to these seven criteria.

1. **Research question**: why the authors do this research and what is its importance and application.
2. **Novelty**: a paper gives new ideas, derivations, applications that have been not studied before or little- or not in depth-studied.
3. **Literature review**: identify the research gap with recent references from 2016 onwards.
4. **Research methodology**: analytical, numerical or experimental or mixed. What is the authors' contribution, assumptions and/or approximations used, description of apparatus and its limitations, steps of experiments, etc.?
5. **Quality of results**: ensure the quality, the depth, and the logic of the discussion.
6. **Insight:** conveyed and recommendations that others might use for future work.
7. **English:** used effectively to communicate the ideas that easy to understand with no grammatical errors or typos.

Assoc. Prof. Dr. Abdulkareem Sh. Mahdi Al-Obaidi, CEng MIMechE

Editor-in-Chief, Journal of Engineering Science & Technology

http://jestec.taylors.edu.my

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2 lampiran

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Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id> 8 November 2022 pukul 07.55
Kepada: Jestec <Jestec@taylors.edu.my>
Cc: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>
Bcc: Amirullah Amirullah <amirullah.ubhara.surabaya@gmail.com>

Dear Prof,
Thanks a lot for sending me this entitled paper.
I will review it before the deadline.

Dr Amirullah,
Power Quality, Power Distribution, Power Electronics, and Renewable Energy base Artificial Intelligent Research,
Universitas Bhayangkara Surabaya Indonesia
[Kutipan teks disembunyikan]

Jestec <Jestec@taylors.edu.my> 8 November 2022 pukul 08.17
Kepada: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Dear Dr Amirullah.

Thank you in advance for the support and accepting the review invitation.

Best regards

Abdulkareem

[Kutipan teks disembunyikan]

Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id> 18 November 2022 pukul 09.48
Kepada: Jestec <Jestec@taylors.edu.my>
Cc: Jestec <Jestec@taylors.edu.my>
Bcc: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Dear Dr Abdulkareem

Here I send you the reviewed paper entitled **EVALUATION OF CHB MLI-BASED SHUNT APF USING LOW PASS FILTER AND SELF-TUNING FILTER.**

Dr Amirullah
Power Quality, Power Electronics, dan Renewable Energy Research
Universitas Bhayangkara Surabaya Indonesia
[Kutipan teks disembunyikan]

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2 lampiran

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Jestec <Jestec@taylors.edu.my> 18 November 2022 pukul 21.23
Kepada: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Dear Dr.

Thank you for your kind email.

We confirm that we received your review report.

We will reply you later with some details.

Best regards

JESTEC Editor

https://jestec.taylors.edu.my

[Kutipan teks disembunyikan]

Jestec <Jestec@taylors.edu.my> 8 Januari 2023 pukul 10.11
Kepada: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Dear Dr.

I would like to express on behalf of the Review panel our sincere thanks for your effort shown in reviewing this paper and your continuous dedication in supporting our journal.

We highly appreciate this effort and support and hope that we may call upon you again to review future manuscripts.

Kindly accept the attached appreciation letter.

Best regards

Assoc. Prof. Dr. Abdulkareem Sh. Mahdi Al-Obaidi, CEng MIMechE

Editor-in-Chief, Journal of Engineering Science & Technology

http://jestec.taylors.edu.my

From: Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>
Sent: Friday, November 18, 2022 10:49 AM
To: Jestec <Jestec@taylors.edu.my>

[Kutipan teks disembunyikan]

[Kutipan teks disembunyikan]

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Lampiran 2

Bukti Pendukung

Journal of Engineering Science and Technology
Vol. XX, No. Y (Year) PPP - QQQ

EVALUATION OF CHB MLI BASED SHUNT APF USING LOW PASS FILTER AND SELF-TUNING FILTER

Abstract

The increasing demand on high rating power supply in distribution system will cause the conventional inverter topology, knows as Six Step Voltage Source Inverter (SSVSI), and is not suitable to be applied as Active Power Filter (APF). In this case, Multilevel Inverter (MLI) is generally the best suitable inverter for APF but not all types of MLI can be uses for high voltage application. Among MLIs, Cascaded H-Bridge (CHB) topology is one if the best choices since it is capable to produce output voltage more than twice amount of DC source. Moreover, CHB MLI topology uses less power devices and simple in design. In its controller Low Pass Filter (LPF) is the common method used in harmonic extraction. This conventional method is facing various problems especially additional need for Phase Lock Loop (PLL) algorithm, slow in transient and steady state responses. A new filtering method is introduced to overcome this problem namely Self Tuning Filter (STF). This paper presents the performance evaluation of CHB MLI for APF using STF as a harmonic extraction. The model has been developed and verified in MATLAB/Simulink. Based on the results, harmonic extraction using STF shows better compare than the conventional LPF and yet both algorithms produce Total Harmonic Distortion (THD) below than 5% as defined as the permissible value stated in IEEE 519.

Keywords: Multilevel Inverter, Shunt Active Power Filter, Total Harmonic Distortion, Self-Tuning Filter, Low Pass Filter

1. Introduction

Power quality is a general term used to represent the interaction of electrical power with electrical equipment. It is defined in the IEEE 100 Authoritative Dictionary of IEEE Standard Term as the concept of powering and grounding sensitive equipment in a manner that is suitable to the operation of that equipment. Since late 1980s power quality problem has become priority in the distribution system. There are three parties that concern about power quality such as utility companies, equipment manufacturers and electric power consumers. The characteristics of the power quality of the AC power system are divided into two, which are Total Harmonic Distortion (THD) and Power Factor (PF) [1]. Besides, there are two power quality terms widely used in power systems. First, it is called as good power quality, which can be used to define a power supply that is always available, consistently within the voltage and frequency tolerance, and then any load connected to it will run smoothly and efficiently. In addition, having a pure noise-free sinusoidal wave shape is one of the characters of the good power quality. Meanwhile, the poor power quality in power system is defined when the load connected to it fails or has a reduced lifetime and efficiency of the electrical installation. Besides, poor power quality can affect the accuracy of utility metering and the equipment in use is vulnerable to damage or service disturbance which will cause maloperation of equipment and premature failure [2-4].

Harmonic distortion is caused by non-linear loads that connected to the power system. It has gaining endless attention due to the increasing of non-linear loads used in daily life. The voltage and current harmonics are coming from power electronic devices. They have been widely used in electrical component such as chopper, rectifier and cyclo-converter. These non-linear loads affect the flow of power by drawing currents only during certain intervals of the fundamental period. When the supplied current is not drawn linearly as in sinusoidal waveform, it will draw higher percentage of harmonic distortion. Harmonic also can be observed when the current not in sinusoidal pattern although the voltage supply is in sine wave. The example of non-linear loads that produce high harmonic distortion are transformers, arc furnaces, variable frequency drives and equipment like computers and copy machines [5-6].

IEEE Standard 519-2014, "IEEE recommended Practice and Requirements for Harmonic Control in Electrical Power System" provides a guide line, limitation and procedures outlined for applying harmonics limits in power systems. This standard is an ordinary standard, which is applied to each type of static power converters used in industrial power systems. It briefly explains the THD of current drawn must be below 5% and harmonic for single component must not exceed than 3%. IEEE 519-2014 will ensure that multiple customers are always producing the less amount of harmonic voltage. However, this standard is not covering the effect of radio frequency interference. In power system, filtering is very important to protect the consumer from an inadequate supply voltage quality. Normally, the nonlinear loads generate harmonic current, distorting the voltage waveform. There are two types of harmonic elimination, which can be done by Passive Power Filter (PPF) and Active Power Filter (APF). PPF is a simple filter that consists of four component made by the passive elements such as capacitance, inductance, damping resistor and transformer. PPF is a filter that has no active component; thus, it does not need additional power supply for its own operation. In addition, previous studies state those PPFs not only filter current components but are also source of reactive power that can be used for compensation [7-8].

The increasing demand on high rating power supply in distribution system will cause the conventional inverter topology, which is Six Step Voltage Source Inverter (SSVSI) (Fig. 1) not suitable for APF. In this case, MLI is the most suitable inverter for APF but not all types of MLI can be used for high voltage application. CHB topology is a better choice than other MLIs because it is capable to produce output voltage more than twice the amount of DC source. Moreover, this topology uses less power device and simple in design. However, on the other hand, CHB topology is facing a key problem on voltage unbalance of DC-link capacitor, which leads to bad performances in process of compensation and unequal stress of semiconductor devices. In additional, more complicated problem occurs by maintaining the voltage of DC-link capacitor if the CHB MLI produces more level of output voltage [9].

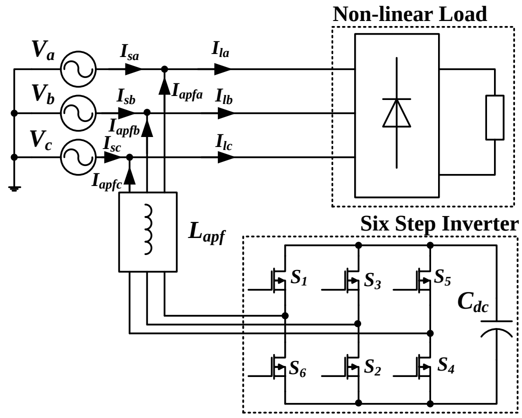


Fig. 1. Conventional six-step inverter based SAPF

Therefore, this paper presents evaluation performance of CHB MLI by using two different type of harmonic extraction namely Low Pass Filter (LPF) and Self-Tuning Filter (STF) used in Shunt APF (SAPF). Both of harmonic extraction will used the same switching algorithms and DC link capacitor algorithms, which are Space Vector Pulse Width Modulation (SVPWM) and PI Controller algorithms respectively. Also, both harmonic extraction algorithms are tested under steady state and dynamic state conditions, where under steady state condition the THD of line current will be compared and under dynamic state condition the transient response will be compared.

2. Multilevel Inverter in SAPF

The multilevel inverter (MLI) has been presented since 1975 as alternative in producing medium and high voltage for several applications. The main purpose of MLI is to synthesize a near sinusoidal voltage from several levels of DC voltages. As the number of levels increases, it will provide a staircase wave that approaches a desired waveform, hence the harmonic distortion of the output wave will be decreased. MLI comes with three types, which are Diode Clamped MLI, Flying Capacitors MLI and Cascaded H-Bridge MLI. Based on current scenario of APF, most are using SSVSI, which is based on six switches and at the same time only capable to be used in low and medium voltage applications. Among MLI, only CHB can operate in high voltage application due to its capability to produce output voltage twice than DC input. The advantages of CHB MLI in high voltage application are transformer less, more economical, capable to produce low harmonic output current, high efficiency for fundamental frequency, capable to work under high switching frequency, and reduce voltage stresses across switches. The increasing number of H-bridges will synthesize output waveform to add more steps in output voltage which can produce a staircase wave to be approaching the sinusoidal wave with minimum harmonic distortion. Fig. 2 shows the CHB MLI configuration in SAPF [10-14].

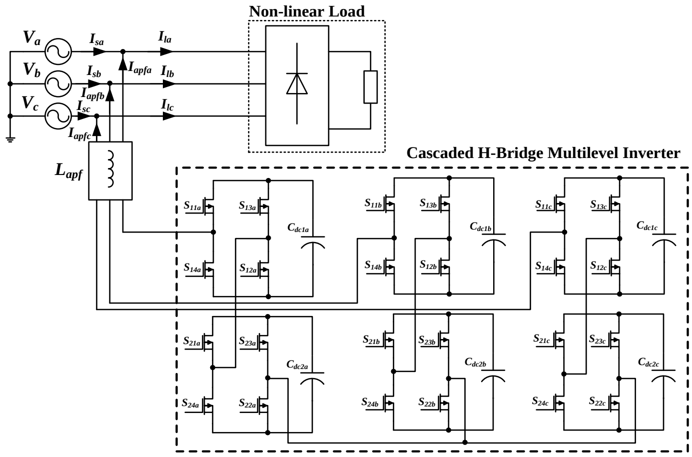


Fig. 2. CHB MLI configuration in SAPF

3. Control Algorithms

There are three main algorithms involved in operation of APF, which are harmonic extraction, DC link capacitor, and switching algorithm. Each algorithm was designed and develop using MATLAB/Simulink tool. Harmonic extraction algorithm, also known as reference current algorithm, intentionally produces the reference signal current (i_{ref}) used to generate the switching signal for inverter. DC link capacitor algorithm is used to maintain voltage at capacitor on certain desired value to make the inverter works as APF, which produces the current injected to the PCC. Fig. 3 shows the control algorithms using different harmonic extraction techniques, which are LPF and STF.

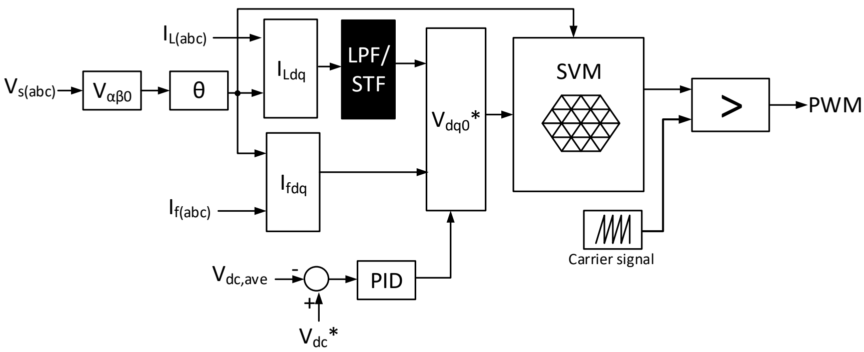


Fig. 3. Low Pass Filter (LPF) and Self Tuning Filter (STF) in SAPF

3.1 Harmonic extraction

The conventional technique used in APF for harmonic extraction algorithm is Low Pass Filter (LPF). The major drawback using LPF is high value of percentage error to be produced in phase and magnitude of the harmonic components, which contribute to mitigation to only high order harmonic components. Due to the drawback of LPF, Self-Tuning Filter (STF) is introduced to overcome the time response issue in transient and steady state conditions in the distribution power system. The advantages of the STF besides working well in steady and transient state conditions, it does not require PLL, no unity gain and phase delay at the fundamental frequency component and easy to implement in digital or analogue control system. The modification of the harmonic extraction from LPF to STF will significantly improve the performance of SAPF

3.1.1 Low Pass Filter (LPF)

The capability of LPF is to allow lower frequency below than a selected cutoff frequency through the filter and block frequencies of higher than the cutoff frequency. The Butterworth LPF is used in this research due to its advantages such as a smooth passband and stopband, working capability in high order and the lowest dispersion characteristic. The transfer function of generalized form of frequency response for n^{th} order Butterworth LPF shows in (1), where n is order of the filter, ω is the passband frequency, ω_c is the cutoff frequency and ε is the maximum passband gain. The quality factor or the damping ratio for Butterworth LPF is set to 0.707. The order of Butterworth LPF can be determined using normalized Butterworth equation as stated in (2), in which the equation uses the real coefficients to be multiplied by the pole pair written in complex conjugates. For the second order Butterworth LPF with the cutoff frequency of 50Hz, the transfer function can be written as stated in (3).

$$H(s) = \frac{1}{\sqrt{1+\varepsilon^2(\frac{\omega}{\omega_c})^{2n}}} \qquad (1)$$

Where,

$$\omega_C = 2\pi f_C$$

$$B_n(s) = \begin{cases} \displaystyle\prod_{k=1}^{\frac{n}{2}} \left[s^2 - 2s\cos\left(\frac{2k+n-1}{2n}\pi\right)+1\right] \; ; \; n = even \\ \displaystyle (s+1)\prod_{k=1}^{\frac{n-1}{2}} \left[s^2 - 2s\cos\left(\frac{2k+n-1}{2n}\pi\right)+1\right] ; n = odd \end{cases} \qquad (2)$$

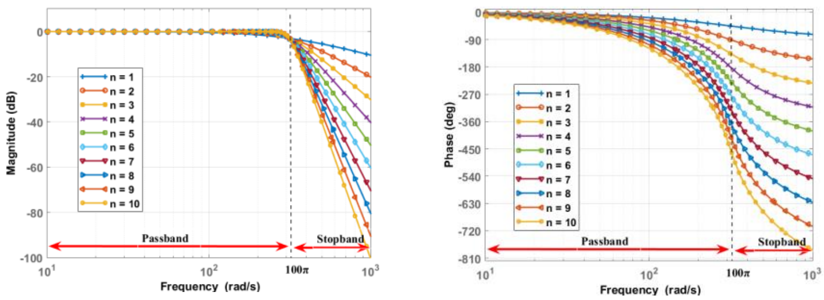
For f_c = 50Hz, ω_c = 312.4 rad/s with n = 2 (even)

$$B_2(s) = \prod_{k=1}^{1} \left[s^2 - 2s\cos\left(\frac{2+2-1}{2(4)}\pi\right)+1\right] = s^2 - 1.414s + 1$$

Transfer function for second order Butterworth

$$H_2(s) = \frac{1}{B_2(s)} | f_c = 50Hz$$
$$H_2(s) = \frac{\omega^2}{s^2 - 1.414\zeta\omega s + \omega^2} = \frac{97594}{s^2 - 312s + 97594} \quad (3)$$

The bode plot frequency response of the Butterworth LPF is shown in Fig. 4 with the order value of n^{th} is set from 1 to 10. The cutoff frequency of the Butterworth LPF is 100π rad/s or equal to 50Hz as the fundamental frequency of supply. Thus, the harmonic component above than the cutoff frequency will be mitigated. Therefore, only harmonic component at the fundamental frequency component will remain. Based on (3) and (4), the increasing of order value of n^{th} in Butterworth LPF will increase the complexity of the transfer function equation even though the shape of magnitude will approach the ideal characteristic of LPF. Thus, this will affect the time response due to calculation process.



(a) **(b)**

Figure 4. Frequency response of Butterworth LPF in SAPF: (a) magnitude and (b) phase

3.1.2 Self Tuning Filter (STF)

Similar function with LPF, STF is used to extract the fundamental component of load current in *d-q* reference frame. Since the load current of *d-q* needs to be filtered the equation of synchronous frame can be written as stated in (4), where $\hat{I}_{dq}(t)$ and $I_{dq}(t)$ represent the instantaneous signals of input and output of the STF filter. By using the Laplace Transformation, (4) can be written as a transfer function stated in (5).

$$\hat{I}_{dq}(t) = e^{j\omega t} \int e^{-j\omega t} I_{dq}(t) dt \quad (4)$$

$$H(s) = \frac{\hat{I}_{dq}(s)}{I_{dq}(s)} = \frac{s + j\omega}{s^2 + \omega^2} \quad (5)$$

The constant *K* needs to be added in (5), in order to limit the magnitude as possible to reach unity value at the cutoff frequency of the transfer function and at the same time phase delay of the transfer function will be equal to zero at the cutoff frequency of the transfer function. The transfer function after adding *K* can be written as

$$H(s) = K\left[\frac{(s+K)+j\omega_c}{(s+K)^2+{\omega_c}^2}\right] = \frac{\hat{I}_{dq}(s)}{I_{dq}(s)} \tag{6}$$

Expression (6) can be expanded into real and imaginary forms as stated in (7), (8) and (9).

$$\frac{\hat{I}_d(s)+j\hat{I}_q(s)}{I_d(s)+jI_q(s)} = K\left[\frac{(s+K)+j\omega_c}{(s+K)^2+{\omega_c}^2}\right] \tag{7}$$

$$\hat{I}_d(s)+j\hat{I}_q(s) = \left(\frac{K(s+K)}{(s+K)^2+{\omega_c}^2}+\frac{jK\omega_c}{(s+K)^2+{\omega_c}^2}\right)\big(I_d(s) + jI_q(s)\big) \tag{8}$$

$$\hat{I}_d(s)+j\hat{I}_q(s) = \frac{K(s+K)}{(s+K)^2+{\omega_c}^2}I_d(s) - \frac{K\omega_c}{(s+K)^2+{\omega_c}^2}I_q(s) + \frac{K(s+K)}{(s+K)^2+{\omega_c}^2}jI_q(s) + \frac{K\omega_c}{(s+K)^2+{\omega_c}^2}jI_d(s) \tag{9}$$

By equating both left and right sides of (9) based on real and imaginary forms, the following expression can be obtained:

$$\hat{I}_d(s) = \frac{K(s+K)}{(s+K)^2+{\omega_c}^2}I_d(s) - \frac{K\omega_c}{(s+K)^2+{\omega_c}^2}I_q(s) \tag{10}$$

$$\hat{I}_q(s) = \frac{K\omega_c}{(s+K)^2+{\omega_c}^2}I_d(s) + \frac{K(s+K)}{(s+K)^2+{\omega_c}^2}I_q(s) \tag{11}$$

By combining (10) and (11), the d-q reference current can be expressed as

$$\begin{bmatrix}\hat{I}_d(s)\\ \hat{I}_q(s)\end{bmatrix} = \frac{K}{(s+K)^2+{\omega_c}^2}\begin{bmatrix}(s+K) & -\omega_c\\ \omega_c & (s+K)\end{bmatrix}\begin{bmatrix}I_d(s)\\ I_q(s)\end{bmatrix} \tag{12}$$

If $\boldsymbol{A} = \begin{bmatrix}(s+K) & -\omega_c\\ \omega_c & (s+K)\end{bmatrix}$ than $|\boldsymbol{A}| = (s+K)^2+{\omega_c}^2$. Hence, (12) can be simplified as

$$\begin{bmatrix}(s+K) & \omega_c\\ \omega_c & (s+K)\end{bmatrix}\begin{bmatrix}\hat{I}_d(s)\\ \hat{I}_q(s)\end{bmatrix} = K\begin{bmatrix}I_d(s)\\ I_q(s)\end{bmatrix} \tag{13}$$

By separating $\hat{I}_d(s)$ and $\hat{I}_q(s)$ component in Equation 13, the equation of $\hat{I}_d(s)$ and $\hat{I}_q(s)$ can be written as shown in (14) and (15). Whereby, $I_d(s)$ and $I_q(s)$ are the input signals meanwhile $\hat{I}_d(s)$ and $\hat{I}_q(s)$ are the output signals from the STF. Fig. 5 shows the detailed block diagram of STF extracted from expression in (14) and (15).

$$\hat{I}_d(s) = \frac{1}{s}\Big(K\big[I_d(s)-\hat{I}_d(s)\big] - \omega_c\hat{I}_q(s)\Big) \tag{14}$$

$$\hat{I}_q(s) = \frac{1}{s}\Big(K\big[I_q(s)-\hat{I}_q(s)\big] - \omega_c\hat{I}_d(s)\Big) \tag{15}$$

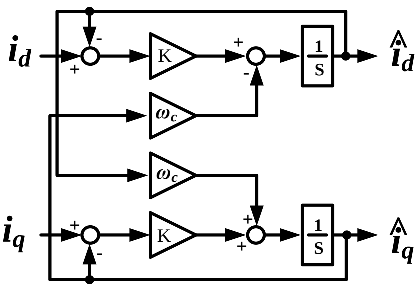
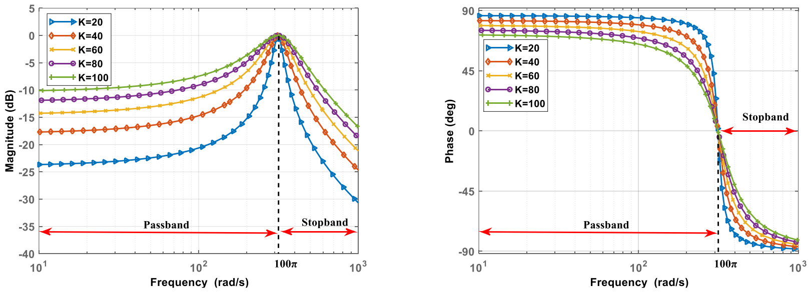


Fig. 5. Block diagram of STF

The constant value *K* or also known as the selectivity parameter will affect performance of the STF as shown in Fig. 6 for range of *K* from 20 to 100. Based on the magnitude and phase of bode plot, the cutoff frequency of the STF is 100π rad/s or equal to 50Hz as the fundamental frequency of supply. Therefore, the harmonic component above than the cutoff frequency will be mitigated and only the fundamental component remains. It is noticeable that the decrement of *K* in phase will make the shape of frequency response to approach the ideal characteristic of STF. By reducing the value of *K*, the fundamental component obtained from the distorted load current will not having phase delay and amplitude change. This is because the smaller value of *K* will increase the filter selectivity in STF.



(a) (b)

Fig. 6. Frequency response of the STF in SAPF: (a) magnitude and (b) phase

3.2 DC Link Capacitor

A DC link capacitor, C_{dc} is used as the storage element of the SAPF, which works continuously in a charged or discharge condition of voltage from power system to the load. The stability of SAPF is depending on ability of voltage balancing algorithms to maintain the DC voltage at the DC link capacitor closer to the reference value of the capacitor voltage. If the voltage below than the reference value SAPF could not operate accordingly to mitigate the harmonics. The instantaneous reference energy of storage $W_{dc,ref}$ shows in (1) based on the instantaneous reference voltage drop across the DC link capacitor $V_{dc,ref}$. The value of DC link capacitor needs to be selected appropriately, in order to control effectively the amplitude voltage fluctuations across DC link capacitor.

$$W_{dc,ref}(t) = \frac{1}{2} C_{dc} V_{dc,ref}^2(t) \tag{16}$$

The change of instantaneous energy of DC link capacitor within period one cycle shows in (17), in which the load current will charge and discharge the DC link capacitor at the steady state condition. Therefore, by using energy balance concept, the charge of the capacitor energy is equal to the reactive and harmonic of the load current as stated in (18). Be rearranging (18), the minimum size of DC link capacitor can be written in (19), where ΔV_{dc} is the maximum or minimum DC bus capacitor voltages, $V_{dc,ref}$ is the DC bus capacitor voltage reference, V_s is the RMS value of source voltage and ΔI_L is the peak RMS value of the reactive and harmonic load current.

$$\Delta W_{dc}(t) = W_{dc,ref}(t) - W_{dc}(t) \tag{17}$$

$$\frac{1}{2} C_{dc}\left[\Delta V_{dc}^2 - \Delta V_{dc,ref}^2\right] = \frac{1}{2}\sqrt{2} V_s \Delta I_L \frac{T}{2} \tag{18}$$

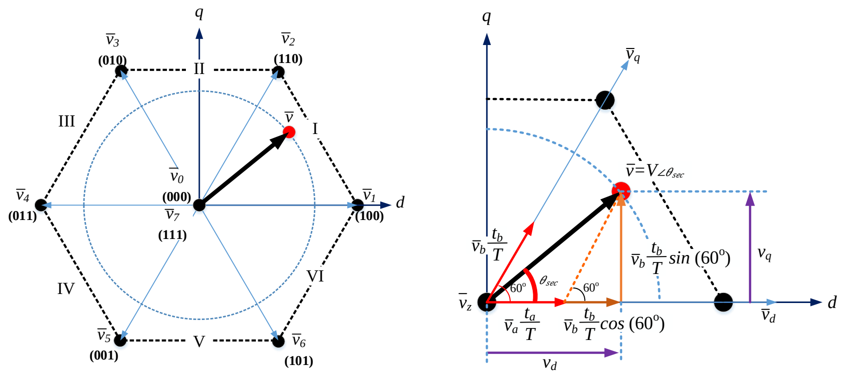
$$C_{dc} \geq \frac{\sqrt{2} V_s \Delta I_L T}{2\left[\Delta V_{dc}^2 - \Delta V_{dc,ref}^2\right]} \tag{19}$$

CHB MLI SAPF for three-phase three-wire system uses six DC-link capacitors, which is controlled by PI controller in each of DC link capacitor connected to each H-Bridge inverter. Let K_p and K_i are set to 0.8 and 8, respectively, so that voltage drop in each capacitor either in the transient and steady state conditions can be controlled. By adding all DC link capacitor, n = 6, which is the total DC link capacitor voltage used in CHB MLI SAPF, hence, the average DC link capacitor voltage can be determined.

$$V_{dc,ave} = \frac{\sum_n V_{dc,n}}{n} \tag{20}$$

3.3 Space Vector Pulse Width Modulation (SVPWM)

SVPWM is generally popular because of several features such as good utilization of DC link voltage and low current ripple. These features make SVPWM suitable for use in high voltage applications. However, this technique is quite complicated due to the process to formulate the sector, table requirements and the switching intervals for all vector positions. Despite of this complexity, the designed algorithm is easy to apply in the hardware implementation. SVPWM is also known as an alternative and popular control method to determine the switching pulse width and their position. The fact that there is a degree of freedom of placement of the space vector in the switching cycle in SVPWM contribute to improve the harmonic performance in MLI. When compared to SPWM, SVPWM obtains better voltage ratio value and can produce greater maximum peak output voltage.



(a) Principle of SVPWM **(b) Resultant space voltage vector**

Fig. 7. Principle of SVPWM

Fig. 7(a) shows the principle of SVPWM representing three-phase output voltage of the inverter illustrated in space vector diagram, which consists of six sectors and the resultant space voltage in sector I. The detailed phasor diagram of the space voltage vector ($\overline{v}$) shown in Fig. 7(b) and can be written in (21), where t_z, t_a and t_b are the respective times for applying zero vector ($\overline{v}_z$), and two adjacent vectors ($\overline{v}_a$ and $\overline{v}_b$). T is the sampling time for one cycle period as stated in (22).

$$\overline{v} = \overline{v}_a\frac{t_a}{T} + \overline{v}_b\frac{t_b}{T} + \overline{v}_z\frac{t_z}{T} \tag{21}$$

$$T = t_a + t_b + t_z \tag{22}$$

Space voltage vector, $\overline{v}$ from (21) can be expressed into a rectangular form as stated in (23), where the voltage components in scalar quantity can be written as stated in (24) and (25).

$$\overline{v} = v_d + jv_q \tag{23}$$

$$v_d = v_a\frac{t_a}{T} + v_b\frac{t_b}{T}\cos(60°) \tag{24}$$

$$v_q = v_b\frac{t_b}{T}\sin(60°) \tag{25}$$

Based on (24) and (25), the voltage components v_d dan v_q that consist of Amplitude, V and Angle, θ_{sec} can be written as

$$v_d = V\cos(\theta_{sec}) \tag{26}$$

$$v_q = V\sin(\theta_{sec}) \tag{27}$$

Hence, from (26) and (27), the simplified forms of Amplitude, V and Angle, θ_{sec} respectively, are given by

$$V = \sqrt{\left(v_d^2 + v_q^2\right)} \tag{28}$$

$$\theta_{sec} = \tan^{-1}\left(\frac{v_d}{v_q}\right) \tag{29}$$

Since, the space voltage vector in sector I, the Angle (θ_{sec}) can be ranging from 0 to $\pi/3$. Based on (24) and (25), and when the adjacent of the voltage vector is equal, the magnitude is given by

$$v_a = v_b = \frac{2}{3}V_{dc} \tag{30}$$

By solving (24), (25) and (30), the on duration for applying voltage vector $\overline{v}_a, \overline{v}_b$ and $\overline{v}_z$can be calculated using (31), (32) and (33) respectively.

$$t_b = \sqrt{3}\frac{v_q}{V_{dc}}T \tag{31}$$

$$t_a = \frac{3T}{2V_{dc}}\left(v_d - \frac{v_q}{\sqrt{3}}\right) \tag{32}$$

$$t_z = T - (t_a + t_b) \tag{33}$$

4. Simulation Results and Analysis

Both of LPF and STF as harmonic extraction algorithms for CHB MLI are designed, developed and verified though MATLAB/Simulink as shown in Fig. 8 based on parameters stated in Table 1. The details of block control algorithms for both of STF and LPF are shown in Fig. 9(a), Fig. 9(b-i) and Fig. 9(b-ii) respectively.

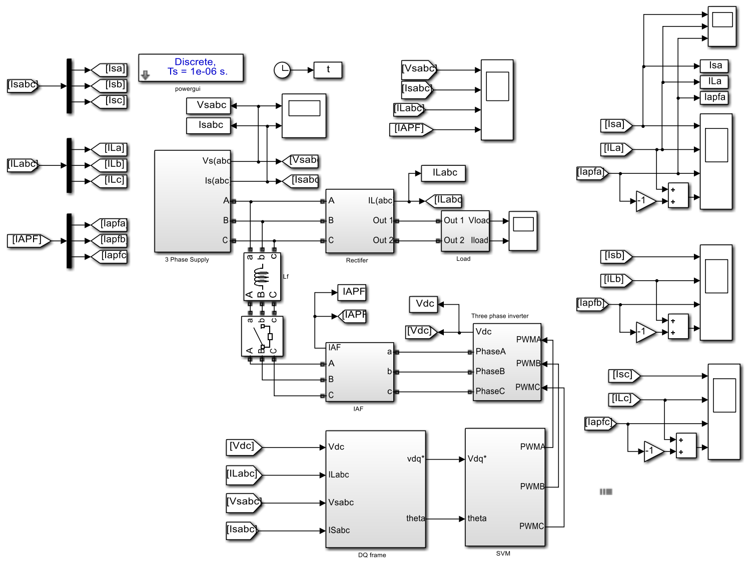


Fig. 8. MATLAB/Simulink simulation model.

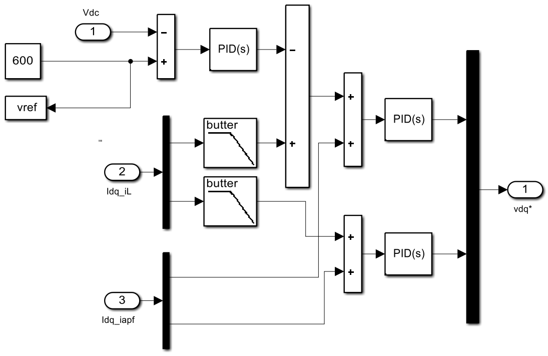
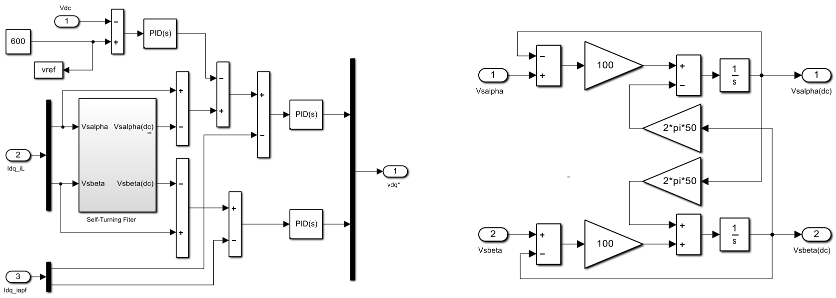


Fig. 9 (a). Simulation model LPF based harmonic extraction.



(i) **(ii)**

Fig. 9 (b). Simulink model of STF based harmonic extraction.

Table 1. Parameters of SAPF

Parameter	***Value***
Voltage source	400 Vrms 50 Hz
Smoothing Inductor, I_{apf}	5 mH
Capacitor Link, C_{dc}	3300 μF 400V (each)
Line Inductor, I_l	2 mH
Switching frequency	20 kHz
Resistive Load	Rectifier + 20 Ω
Inductive Load	Rectifier + 50 mH (Series with 20 Ω)
Capacitive Load	Rectifier + 100 μF (Parallel with 20 Ω)

The voltage supply for this experiment is using balanced sinusoidal source voltage as stated in expression below.

$$V_{an} = 326 \sin 100\pi t \tag{34}$$

$$V_{bn} = 326 \sin(100\pi t - 120°) \tag{35}$$

$$V_{cn} = 326 \sin(100\pi t + 120°) \tag{36}$$

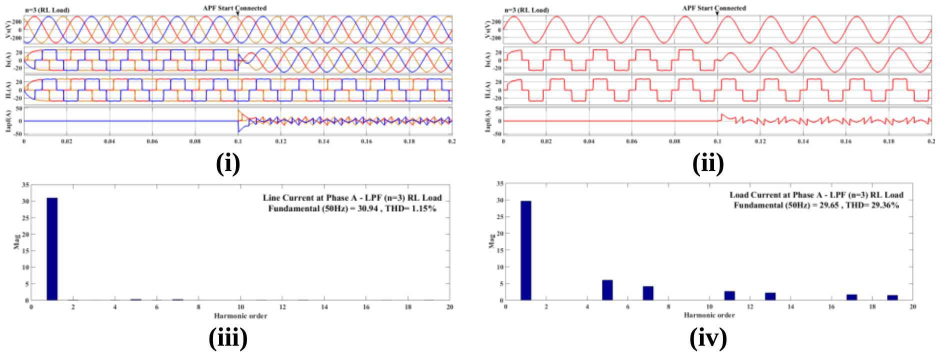


Fig. 10. LPF based harmonic extraction for inductive load at *n*=3: (i) three-phase line voltage, three-phase line current, three-phase load current and three-phase APF current, (ii) voltage and current at Phase A, (iii) THD of line current at Phase A and (iv) THD of load current at Phase A.

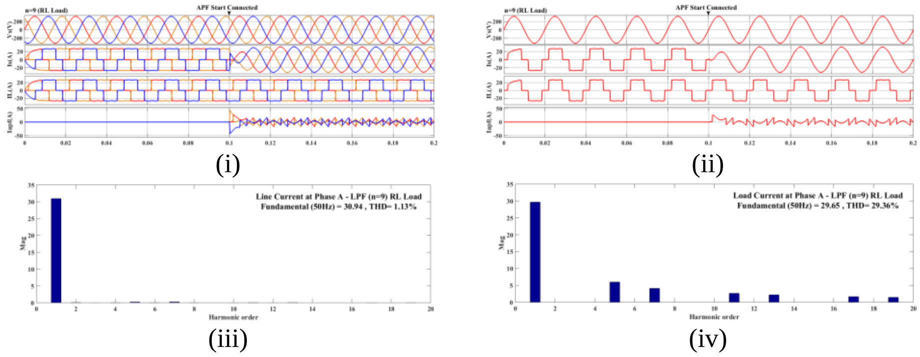


Fig. 11. LPF based harmonic extraction for inductive load at *n* = 9: (i) three-phase line voltage, three-phase line current, three-phase load current and three-phase APF current, (ii) voltage and current at Phase A, (iii) THD of line current at Phase A (iv) THD of load current at Phase A.

Fig. 10 and Fig. 11 show the results obtained according to LPF based harmonic extraction method for inductive load at filter order *n* of 3 and 9. Based on the results, THD for $n = 3$ reduces from 29.36% (load current) to 1.15% (line current). Meanwhile, for $n = 9$, the THD drops form 29.36% (line current) to 1.13% (line current). The highest number of *n* will perform better mitigation of harmonics due to load current.

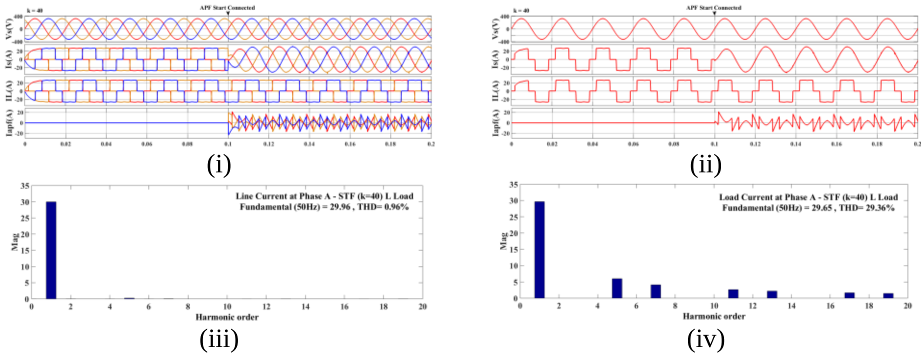


Fig. 12. STF based harmonic extraction for inductive load at *K*=40: (i) three-phase line voltage, three-phase line current, three-phase load current and three-phase APF current, (ii) voltage and current at Phase A, (iii) THD of line current at Phase A and (iv) THD of load current at Phase A.

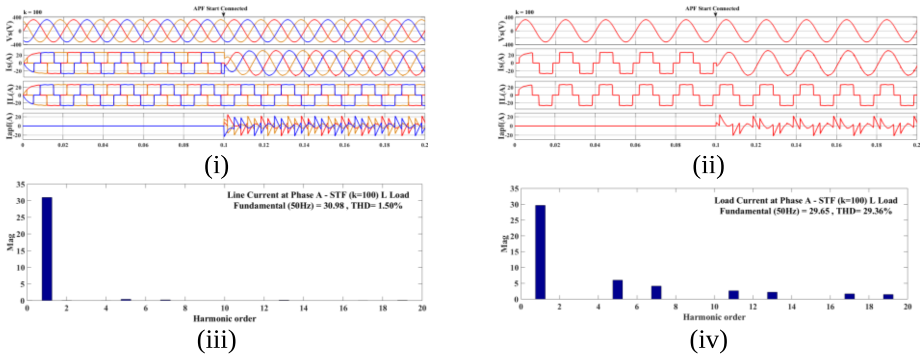


Fig.13. STF harmonic extraction for Inductive load at *K*=100: (i) three-phase line voltage, three-phase line current, three-phase load current and three-phase APF current, (ii) voltage and current at Phase A, (iii) THD of line current at Phase A and (iv) THD of load current at Phase A.

Fig. 12 and Fig. 13 show the results obtained according to STF based harmonic extraction method for inductive load at selective parameter *K* 40 and 100. Based on the results, THD for *K*=40 reduces from 29.36% (load current) to 0.96% (line current). Meanwhile, for *K*=100 the THD drops from 29.36% (load current) to 1.50% (line current). The lowest number of *K* will perform better mitigation of harmonics due to the load current.

In additional, both of LPF and STF based harmonic extraction methods are tested with several of load, *n* for LPF and *K* for STF. The summarized performance of both algorithms are tabulated in Table 2 and Table 3 respectively. From Table 2, the increased value of *n* in LPF will produce better percentage of THD of line current for all tested loads. Meanwhile for Table 3, the decreased value of *K* in STF will produce better percentage of THD of line current for all tested loads.

Table 2. Performance of LPF with several loads

Load	LPF (THD of line and load current)														
	n = 1			n = 3			n = 5			n = 7			n = 9		
	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%
Resistive	29.47	3.98	86.5	29.47	1.53	94.8	29.47	1.50	94.9	29.47	1.50	94.9	29.47	1.50	94.9
Inductive	29.36	4.07	86.1	29.36	1.15	96.1	29.36	1.14	96.1	29.36	1.13	96.2	29.36	1.13	96.2
Capacitive	55.01	4.37	92.1	55.01	3.11	94.3	55.01	3.05	94.5	55.01	3.05	94.5	55.01	3.05	94.5

Table 3. Performance of STF with several loads

Load	STF algorithm technique (THD of line and load current)														
	K = 20			K = 40			K = 60			K = 80			K = 100		
	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%
Resistive	29.47	1.34	95.5	29.47	1.36	95.4	29.47	1.45	95.1	29.47	1.58	94.6	29.47	1.75	94.1
Inductive	29.36	0.93	96.8	29.36	0.96	96.7	29.36	1.09	96.3	29.36	1.29	95.6	29.36	1.5	94.9
Capacitive	32.51	1.59	95.1	32.51	1.72	94.7	32.51	1.87	94.2	32.51	2.05	93.7	32.51	2.25	93.1

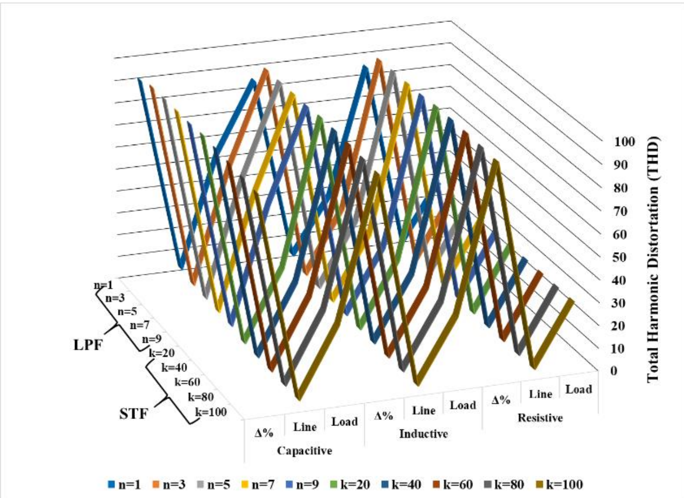


Fig. 14. Percentage reduction of THD of current for LPF and STF algorithms

Fig. 14 shows the percentage reduction of THD of line current for both LPF and STF algorithms. Both algorithms are capable to mitigate more than 85% of THD of load current. The high value of order in LPF contributes less value of THD, due to that the higher order will produce frequency response approaching to the ideal frequency response of LPF as shown early in Figure 4. In other words, the effect of higher order will shift the roll-off frequency response near to the ideal shape of LPF with angle perpendicular to 90°. However, the high order may cause the equation become more complex which contributes to increment of calculation time in the processor.

5. Conclusion

This paper demonstrates the performances of LPF and STF based harmonic extraction algorithms in CHB MLI SAPF. To obtain better percentage of THD of line current, the filter's order needs to be increased in LPF based harmonic extractions; meanwhile, the value of selective parameter needs to be decreased in STF based harmonic extraction. Based on the simulation results, both harmonic extractions have successfully operated CHB MLI SAPF with THD to be below 5%, as to follow the IEEE 519 Standard. STF based harmonic extraction is capable of mitigate more THD in load current compare to LPF based harmonic extraction. To achieve same performance as STF, the LPF needs to perform with high-order complex mathematical equations that contribute to creating time delay and at the same time, decreasing performance of SAPF. Implementing high order of LPF based harmonic extraction in hardware development is even more difficult.

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EVALUATION OF CHB MLI BASED SHUNT APF USING LOW PASS FILTER AND SELF-TUNING FILTER

Abstract

The increasing demand on high rating power supply in distribution system will cause the conventional inverter topology, knows as Six Step Voltage Source Inverter (SSVSI), and is not suitable to be applied as Active Power Filter (APF). In this case, Multilevel Inverter (MLI) is generally the best suitable inverter for APF but not all types of MLI can be uses for high voltage application. Among MLIs, Cascaded H-Bridge (CHB) topology is one if the best choices since it is capable to produce output voltage more than twice amount of DC source. Moreover, CHB MLI topology uses less power devices and simple in design. In its controller Low Pass Filter (LPF) is the common method used in harmonic extraction. This conventional method is facing various problems especially additional need for Phase Lock Loop (PLL) algorithm, slow in transient and steady state responses. A new filtering method is introduced to overcome this problem namely Self Tuning Filter (STF). This paper presents the performance evaluation of CHB MLI for APF using STF as a harmonic extraction. The model has been developed and verified in MATLAB/Simulink. Based on the results, harmonic extraction using STF shows better compare than the conventional LPF and yet both algorithms produce Total Harmonic Distortion (THD) below than 5% as defined as the permissible value stated in IEEE 519.

Keywords: Multilevel Inverter, Shunt Active Power Filter, Total Harmonic Distortion, Self-Tuning Filter, Low Pass Filter

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1. Introduction

Power quality is a general term used to represent the interaction of electrical power with electrical equipment. It is defined in the IEEE 100 Authoritative Dictionary of IEEE Standard Term as the concept of powering and grounding sensitive equipment in a manner that is suitable to the operation of that equipment. Since late 1980s power quality problem has become priority in the distribution system. There are three parties that concern about power quality such as utility companies, equipment manufacturers and electric power consumers. The characteristics of the power quality of the AC power system are divided into two, which are Total Harmonic Distortion (THD) and Power Factor (PF) [1]. Besides, there are two power quality terms widely used in power systems. First, it is called as good power quality, which can be used to define a power supply that is always available, consistently within the voltage and frequency tolerance, and then any load connected to it will run smoothly and efficiently. In addition, having a pure noise-free sinusoidal wave shape is one of the characters of the good power quality. Meanwhile, the poor power quality in power system is defined when the load connected to it fails or has a reduced lifetime and efficiency of the electrical installation. Besides, poor power quality can affect the accuracy of utility metering and the equipment in use is vulnerable to damage or service disturbance which will cause maloperation of equipment and premature failure [2-4].

Harmonic distortion is caused by non-linear loads that connected to the power system. It has gaining endless attention due to the increasing of non-linear loads used in daily life. The voltage and current harmonics are coming from power electronic devices. They have been widely used in electrical component such as chopper, rectifier and cyclo-converter. These non-linear loads affect the flow of power by drawing currents only during certain intervals of the fundamental period. When the supplied current is not drawn linearly as in sinusoidal waveform, it will draw higher percentage of harmonic distortion. Harmonic also can be observed when the current not in sinusoidal pattern although the voltage supply is in sine wave. The example of non-linear loads that produce high harmonic distortion are transformers, arc furnaces, variable frequency drives and equipment like computers and copy machines [5-6].

IEEE Standard 519-2014, “IEEE recommended Practice and Requirements for Harmonic Control in Electrical Power System” provides a guide line, limitation and procedures outlined for applying harmonics limits in power systems. This standard is an ordinary standard, which is applied to each type of static power converters used in industrial power systems. It briefly explains the THD of current drawn must be below 5% and harmonic for single component must not exceed than 3%. IEEE 519-2014 will ensure that multiple customers are always producing the less amount of harmonic voltage. However, this standard is not covering the effect of radio frequency interference. In power system, filtering is very important to protect the consumer from an inadequate supply voltage quality. Normally, the nonlinear loads generate harmonic current, distorting the voltage waveform. There are two types of harmonic elimination, which can be done by Passive Power Filter (PPF) and Active Power Filter (APF). PPF is a simple filter that consists of four component made by the passive elements such as capacitance, inductance, damping resistor and transformer. PPF is a filter that has no active component; thus, it does not need additional power supply for its own operation. In addition, previous studies state those PPFs not only filter current components but are also source of reactive power that can be used for compensation [7-8].

The increasing demand on high rating power supply in distribution system will cause the conventional inverter topology, which is Six Step Voltage Source Inverter (SSVSI) (Fig. 1) not suitable for APF. In this case, MLI is the most suitable inverter for APF but not all types of MLI can be used for high voltage application. CHB topology is a better choice than other MLIs because it is capable to produce output voltage more than twice the amount of DC source. Moreover, this topology uses less power device and simple in design. However, on the other hand, CHB topology is facing a key problem on voltage unbalance of DC-link capacitor, which leads to bad performances in process of compensation and unequal stress of semiconductor devices. In additional, more complicated problem occurs by maintaining the voltage of DC-link capacitor if the CHB MLI produces more level of output voltage [9].

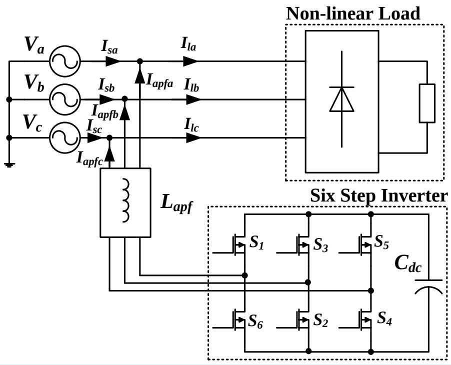

Fig. 1. Conventional six-step inverter based SAPF

Therefore, this paper presents evaluation performance of CHB MLI by using two different type of harmonic extraction namely Low Pass Filter (LPF) and Self-Tuning Filter (STF) used in Shunt APF (SAPF). Both of harmonic extraction will used the same switching algorithms and DC link capacitor algorithms, which are Space Vector Pulse Width Modulation (SVPWM) and PI Controller algorithms respectively. Also, both harmonic extraction algorithms are tested under steady state and dynamic state conditions, where under steady state condition the THD of line current will be compared and under dynamic state condition the transient response will be compared.

2. Multilevel Inverter in SAPF

The multilevel inverter (MLI) has been presented since 1975 as alternative in producing medium and high voltage for several applications. The main purpose of MLI is to synthesize a near sinusoidal voltage from several levels of DC voltages. As the number of levels increases, it will provide a staircase wave that approaches a desired waveform, hence the harmonic distortion of the output wave will be decreased. MLI comes with three types, which are Diode Clamped MLI, Flying Capacitors MLI and Cascaded H-Bridge MLI. Based on current scenario of APF, most are using SSVSI, which is based on six switches and at the same time only

Commented [WU2]: 2.Enlarge Fig 1 to the right and left ends of the paper page.

Commented [WU3]: 3.After this paragraph in the introductory section, briefly explain the parts of the discussion in the paper for example section 2 discusses...., section 3 discusses...... until the last section to provide an initial explanation to the reader about a brief description of the contents of the paper.

Commented [WU4]: 4.Move the title of sub-chapter 2 Multilevel Inverter in SAPF to sub-chapter 3.1 after sub-chapter 3. Proposed method capable to be used in low and medium voltage applications. Among MLI, only CHB can operate in high voltage application due to its capability to produce output voltage twice than DC input. The advantages of CHB MLI in high voltage application are transformer less, more economical, capable to produce low harmonic output current, high efficiency for fundamental frequency, capable to work under high switching frequency, and reduce voltage stresses across switches. The increasing number of H-bridges will synthesize output waveform to add more steps in output voltage which can produce a staircase wave to be approaching the sinusoidal wave with minimum harmonic distortion. Fig. 2 shows the CHB MLI configuration in SAPF [10-14].

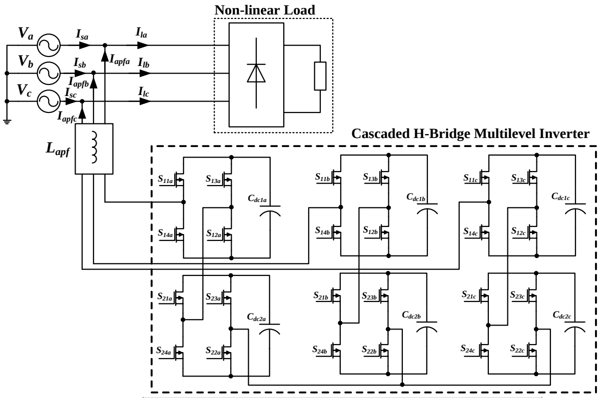

Fig. 2. CHB MLI configuration in SAPF

3. Control Algorithms

There are three main algorithms involved in operation of APF, which are harmonic extraction, DC link capacitor, and switching algorithm. Each algorithm was designed and develop using MATLAB/Simulink tool. Harmonic extraction algorithm, also known as reference current algorithm, intentionally produces the reference signal current (i_{ref}) used to generate the switching signal for inverter. DC link capacitor algorithm is used to maintain voltage at capacitor on certain desired value to make the inverter works as APF, which produces the current injected to the PCC. Fig. 3 shows the control algorithms using different harmonic extraction techniques, which are LPF and STF.

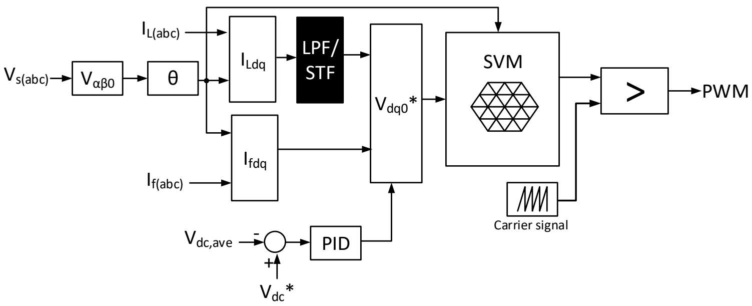

Fig. 3. Low Pass Filter (LPF) and Self Tuning Filter (STF) in SAPF

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3.1 Harmonic extraction

The conventional technique used in APF for harmonic extraction algorithm is Low Pass Filter (LPF). The major drawback using LPF is high value of percentage error to be produced in phase and magnitude of the harmonic components, which contribute to mitigation to only high order harmonic components. Due to the drawback of LPF, Self-Tuning Filter (STF) is introduced to overcome the time response issue in transient and steady state conditions in the distribution power system. The advantages of the STF besides working well in steady and transient state conditions, it does not require PLL, no unity gain and phase delay at the fundamental frequency component and easy to implement in digital or analogue control system. The modification of the harmonic extraction from LPF to STF will significantly improve the performance of SAPF

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3.1.1 Low Pass Filter (LPF)

The capability of LPF is to allow lower frequency below than a selected cutoff frequency through the filter and block frequencies of higher than the cutoff frequency. The Butterworth LPF is used in this research due to its advantages such as a smooth passband and stopband, working capability in high order and the lowest dispersion characteristic. The transfer function of generalized form of frequency response for n^{th} order Butterworth LPF shows in (1), where n is order of the filter, ω is the passband frequency, ω_c is the cutoff frequency and ε is the maximum passband gain. The quality factor or the damping ratio for Butterworth LPF is set to 0.707. The order of Butterworth LPF can be determined using normalized Butterworth equation as stated in (2), in which the equation uses the real coefficients to be multiplied by the pole pair written in complex conjugates. For the second order Butterworth LPF with the cutoff frequency of 50Hz, the transfer function can be written as stated in (3).

$$H(s) = \frac{1}{\sqrt{1+\varepsilon^2(\frac{\omega}{\omega_c})^{2n}}} \qquad (1)$$

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Where,

$$\omega_C = 2\pi f_C$$

$$B_n(s) = \begin{cases} \prod_{k=1}^{\frac{n}{2}} \left[s^2 - 2s\cos\left(\frac{2k+n-1}{2n}\pi\right)+1\right] \; ; \; n = even \\ (s+1)\prod_{k=1}^{\frac{n-1}{2}} \left[s^2 - 2s\cos\left(\frac{2k+n-1}{2n}\pi\right)+1\right] ; n = odd \end{cases} \qquad (2)$$

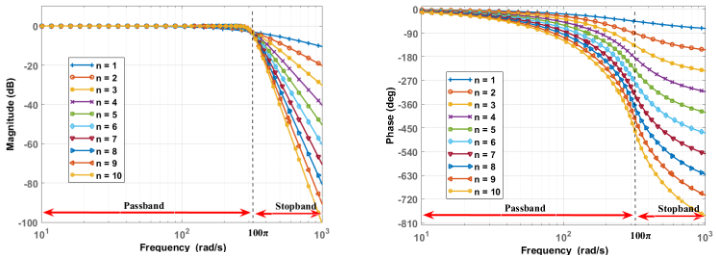
For f_c = 50Hz, ω_c = 312.4 rad/s with n = 2 (even)

$$B_2(s) = \prod_{k=1}^{1} \left[s^2 - 2s\cos\left(\frac{2+2-1}{2(4)}\pi\right)+1\right] = s^2 - 1.414s + 1$$

Transfer function for second order Butterworth

$$H_2(s) = \frac{1}{B_2(s)} | f_c = 50Hz$$
$$H_2(s) = \frac{\omega^2}{s^2 - 1.414\zeta\omega s + \omega^2} = \frac{97594}{s^2 - 312s + 97594} \quad (3)$$

The bode plot frequency response of the Butterworth LPF is shown in Fig. 4 with the order value of n^{th} is set from 1 to 10. The cutoff frequency of the Butterworth LPF is 100π rad/s or equal to 50Hz as the fundamental frequency of supply. Thus, the harmonic component above than the cutoff frequency will be mitigated. Therefore, only harmonic component at the fundamental frequency component will remain. Based on (3) and (4), the increasing of order value of n^{th} in Butterworth LPF will increase the complexity of the transfer function equation even though the shape of magnitude will approach the ideal characteristic of LPF. Thus, this will affect the time response due to calculation process.



(a) **(b)**

Figure 4. Frequency response of Butterworth LPF in SAPF: (a) magnitude and (b) phase

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3.1.2 Self Tuning Filter (STF)

Similar function with LPF, STF is used to extract the fundamental component of load current in *d-q* reference frame. Since the load current of *d-q* needs to be filtered the equation of synchronous frame can be written as stated in (4), where $\hat{I}_{dq}(t)$ and $I_{dq}(t)$ represent the instantaneous signals of input and output of the STF filter. By using the Laplace Transformation, (4) can be written as a transfer function stated in (5).

$$\hat{I}_{dq}(t) = e^{j\omega t} \int e^{-j\omega t} I_{dq}(t) dt \quad (4)$$

$$H(s) = \frac{\hat{I}_{dq}(s)}{I_{dq}(s)} = \frac{s + j\omega}{s^2 + \omega^2} \quad (5)$$

The constant *K* needs to be added in (5), in order to limit the magnitude as possible to reach unity value at the cutoff frequency of the transfer function and at the same time phase delay of the transfer function will be equal to zero at the cutoff frequency of the transfer function. The transfer function after adding *K* can be written as

$$H(s) = K\left[\frac{(s+K)+j\omega_c}{(s+K)^2+{\omega_c}^2}\right] = \frac{\hat{I}_{dq}(s)}{I_{dq}(s)} \tag{6}$$

Expression (6) can be expanded into real and imaginary forms as stated in (7), (8) and (9).

$$\frac{\hat{I}_d(s)+j\hat{I}_q(s)}{I_d(s)+jI_q(s)} = K\left[\frac{(s+K)+j\omega_c}{(s+K)^2+{\omega_c}^2}\right] \tag{7}$$

$$\hat{I}_d(s)+j\hat{I}_q(s) = \left(\frac{K(s+K)}{(s+K)^2+{\omega_c}^2} + \frac{jK\omega_c}{(s+K)^2+{\omega_c}^2}\right)\big(I_d(s) + jI_q(s)\big) \tag{8}$$

$$\hat{I}_d(s)+j\hat{I}_q(s) = \frac{K(s+K)}{(s+K)^2+{\omega_c}^2}I_d(s) - \frac{K\omega_c}{(s+K)^2+{\omega_c}^2}I_q(s) + \frac{K(s+K)}{(s+K)^2+{\omega_c}^2}jI_q(s) + \frac{K\omega_c}{(s+K)^2+{\omega_c}^2}jI_d(s) \tag{9}$$

By equating both left and right sides of (9) based on real and imaginary forms, the following expression can be obtained:

$$\hat{I}_d(s) = \frac{K(s+K)}{(s+K)^2+{\omega_c}^2}I_d(s) - \frac{K\omega_c}{(s+K)^2+{\omega_c}^2}I_q(s) \tag{10}$$

$$\hat{I}_q(s) = \frac{K\omega_c}{(s+K)^2+{\omega_c}^2}I_d(s) + \frac{K(s+K)}{(s+K)^2+{\omega_c}^2}I_q(s) \tag{11}$$

By combining (10) and (11), the d-q reference current can be expressed as

$$\begin{bmatrix}\hat{I}_d(s)\\ \hat{I}_q(s)\end{bmatrix} = \frac{K}{(s+K)^2+{\omega_c}^2}\begin{bmatrix}(s+K) & -\omega_c\\ \omega_c & (s+K)\end{bmatrix}\begin{bmatrix}I_d(s)\\ I_q(s)\end{bmatrix} \tag{12}$$

If $\boldsymbol{A} = \begin{bmatrix}(s+K) & -\omega_c\\ \omega_c & (s+K)\end{bmatrix}$ than $|\boldsymbol{A}| = (s+K)^2 + {\omega_c}^2$. Hence, (12) can be simplified as

$$\begin{bmatrix}(s+K) & \omega_c\\ \omega_c & (s+K)\end{bmatrix}\begin{bmatrix}\hat{I}_d(s)\\ \hat{I}_q(s)\end{bmatrix} = K\begin{bmatrix}I_d(s)\\ I_q(s)\end{bmatrix} \tag{13}$$

By separating $\hat{I}_d(s)$ and $\hat{I}_q(s)$ component in Equation 13, the equation of $\hat{I}_d(s)$ and $\hat{I}_q(s)$ can be written as shown in (14) and (15). Whereby, $I_d(s)$ and $I_q(s)$ are the input signals meanwhile $\hat{I}_d(s)$ and $\hat{I}_q(s)$ are the output signals from the STF. Fig. 5 shows the detailed block diagram of STF extracted from expression in (14) and (15).

$$\hat{I}_d(s) = \frac{1}{s}\Big(K\big[I_d(s) - \hat{I}_d(s)\big] - \omega_c\hat{I}_q(s)\Big) \tag{14}$$

$$\hat{I}_q(s) = \frac{1}{s}\Big(K\big[I_q(s) - \hat{I}_q(s)\big] - \omega_c\hat{I}_d(s)\Big) \tag{15}$$

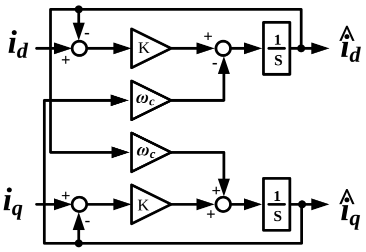
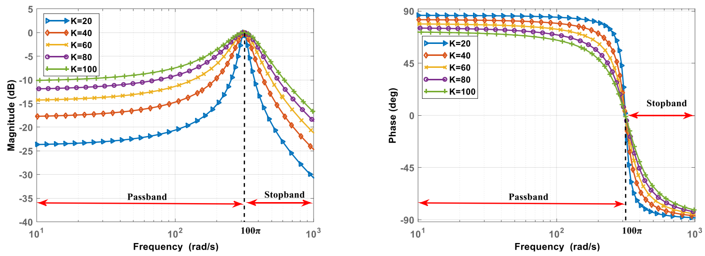


Fig. 5. Block diagram of STF

The constant value *K* or also known as the selectivity parameter will affect performance of the STF as shown in Fig. 6 for range of *K* from 20 to 100. Based on the magnitude and phase of bode plot, the cutoff frequency of the STF is 100π rad/s or equal to 50Hz as the fundamental frequency of supply. Therefore, the harmonic component above than the cutoff frequency will be mitigated and only the fundamental component remains. It is noticeable that the decrement of *K* in phase will make the shape of frequency response to approach the ideal characteristic of STF. By reducing the value of *K*, the fundamental component obtained from the distorted load current will not having phase delay and amplitude change. This is because the smaller value of *K* will increase the filter selectivity in STF.



(a) **(b)**

Fig. 6. Frequency response of the STF in SAPF: (a) magnitude and (b) phase

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3.2 DC Link Capacitor

A DC link capacitor, C_{dc} is used as the storage element of the SAPF, which works continuously in a charged or discharge condition of voltage from power system to the load. The stability of SAPF is depending on ability of voltage balancing algorithms to maintain the DC voltage at the DC link capacitor closer to the reference value of the capacitor voltage. If the voltage below than the reference value SAPF could not operate accordingly to mitigate the harmonics. The instantaneous reference energy of storage $W_{dc,ref}$ shows in (1) based on the instantaneous reference voltage drop across the DC link capacitor $V_{dc,ref}$. The value of DC link capacitor needs to be selected appropriately, in order to control effectively the amplitude voltage fluctuations across DC link capacitor.

$$W_{dc,ref}(t) = \frac{1}{2} C_{dc} V_{dc,ref}^2(t) \tag{16}$$

The change of instantaneous energy of DC link capacitor within period one cycle shows in (17), in which the load current will charge and discharge the DC link capacitor at the steady state condition. Therefore, by using energy balance concept, the charge of the capacitor energy is equal to the reactive and harmonic of the load current as stated in (18). Be rearranging (18), the minimum size of DC link capacitor can be written in (19), where ΔV_{dc} is the maximum or minimum DC bus capacitor voltages, $V_{dc,ref}$ is the DC bus capacitor voltage reference, V_s is the RMS value of source voltage and ΔI_L is the peak RMS value of the reactive and harmonic load current.

$$\Delta W_{dc}(t) = W_{dc,ref}(t) - W_{dc}(t) \tag{17}$$

$$\frac{1}{2} C_{dc}\left[\Delta V_{dc}^2 - \Delta V_{dc,ref}^2\right] = \frac{1}{2}\sqrt{2} V_s \Delta I_L \frac{T}{2} \tag{18}$$

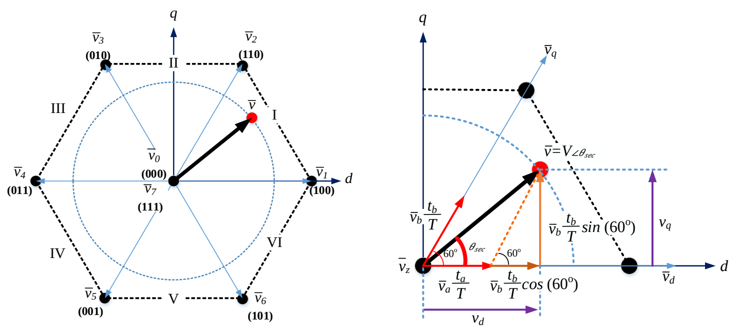
$$C_{dc} \geq \frac{\sqrt{2} V_s \Delta I_L T}{2\left[\Delta V_{dc}^2 - \Delta V_{dc,ref}^2\right]} \tag{19}$$

CHB MLI SAPF for three-phase three-wire system uses six DC-link capacitors, which is controlled by PI controller in each of DC link capacitor connected to each H-Bridge inverter. Let K_p and K_i are set to 0.8 and 8, respectively, so that voltage drop in each capacitor either in the transient and steady state conditions can be controlled. By adding all DC link capacitor, n = 6, which is the total DC link capacitor voltage used in CHB MLI SAPF, hence, the average DC link capacitor voltage can be determined.

$$V_{dc,ave} = \frac{\sum_n V_{dc,n}}{n} \tag{20}$$

3.3 Space Vector Pulse Width Modulation (SVPWM)

SVPWM is generally popular because of several features such as good utilization of DC link voltage and low current ripple. These features make SVPWM suitable for use in high voltage applications. However, this technique is quite complicated due to the process to formulate the sector, table requirements and the switching intervals for all vector positions. Despite of this complexity, the designed algorithm is easy to apply in the hardware implementation. SVPWM is also known as an alternative and popular control method to determine the switching pulse width and their position. The fact that there is a degree of freedom of placement of the space vector in the switching cycle in SVPWM contribute to improve the harmonic performance in MLI. When compared to SPWM, SVPWM obtains better voltage ratio value and can produce greater maximum peak output voltage.



(a) Principle of SVPWM **(b) Resultant space voltage vector**

Fig. 7. Principle of SVPWM

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Fig. 7(a) shows the principle of SVPWM representing three-phase output voltage of the inverter illustrated in space vector diagram, which consists of six sectors and the resultant space voltage in sector I. The detailed phasor diagram of the space voltage vector ($\overline{v}$) shown in Fig. 7(b) and can be written in (21), where t_z, t_a and t_b are the respective times for applying zero vector ($\overline{v}_z$), and two adjacent vectors ($\overline{v}_a$ and $\overline{v}_b$). T is the sampling time for one cycle period as stated in (22).

$$\overline{v} = \overline{v}_a \frac{t_a}{T} + \overline{v}_b \frac{t_b}{T} + \overline{v}_z \frac{t_z}{T} \tag{21}$$

$$T = t_a + t_b + t_z \tag{22}$$

Space voltage vector, $\overline{v}$ from (21) can be expressed into a rectangular form as stated in (23), where the voltage components in scalar quantity can be written as stated in (24) and (25).

$$\overline{v} = v_d + jv_q \tag{23}$$

$$v_d = v_a \frac{t_a}{T} + v_b \frac{t_b}{T} \cos(60°) \tag{24}$$

$$v_q = v_b \frac{t_b}{T} \sin(60°) \tag{25}$$

Based on (24) and (25), the voltage components v_d dan v_q that consist of Amplitude, V and Angle, θ_{sec} can be written as

$$v_d = V\cos(\theta_{sec}) \tag{26}$$

$$v_q = V\sin(\theta_{sec}) \tag{27}$$

Hence, from (26) and (27), the simplified forms of Amplitude, V and Angle, θ_{sec} respectively, are given by

$$V = \sqrt{(v_d^2 + v_q^2)} \tag{28}$$

$$\theta_{sec} = \tan^{-1}\left(\frac{v_d}{v_q}\right) \tag{29}$$

Since, the space voltage vector in sector I, the Angle (θ_{sec}) can be ranging from 0 to $\pi/3$. Based on (24) and (25), and when the adjacent of the voltage vector is equal, the magnitude is given by

$$v_a = v_b = \frac{2}{3}V_{dc} \tag{30}$$

By solving (24), (25) and (30), the on duration for applying voltage vector $\overline{v}_a, \overline{v}_b$ and $\overline{v}_z$can be calculated using (31), (32) and (33) respectively.

$$t_b = \sqrt{3}\frac{v_q}{V_{dc}}T \tag{31}$$

$$t_a = \frac{3T}{2V_{dc}}\left(v_d - \frac{v_q}{\sqrt{3}}\right) \tag{32}$$

$$t_z = T - (t_a + t_b) \tag{33}$$

4. Simulation Results and Analysis

Both of LPF and STF as harmonic extraction algorithms for CHB MLI are designed, developed and verified though MATLAB/Simulink as shown in Fig. 8 based on parameters stated in Table 1. The details of block control algorithms for both of STF and LPF are shown in Fig. 9(a), Fig. 9(b-i) and Fig. 9(b-ii) respectively.

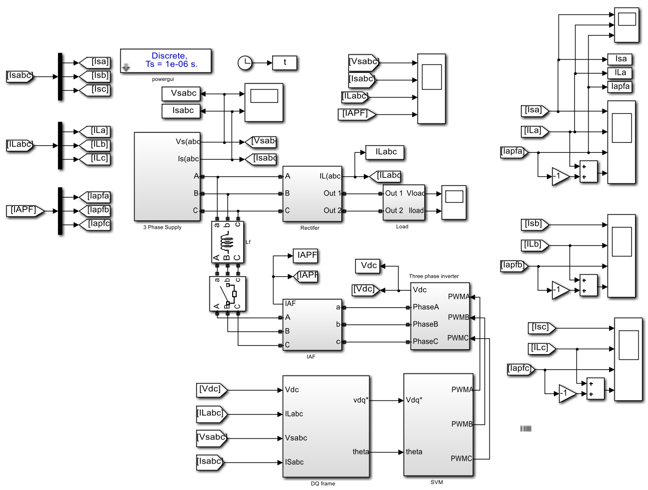

Fig. 8. MATLAB/Simulink simulation model.

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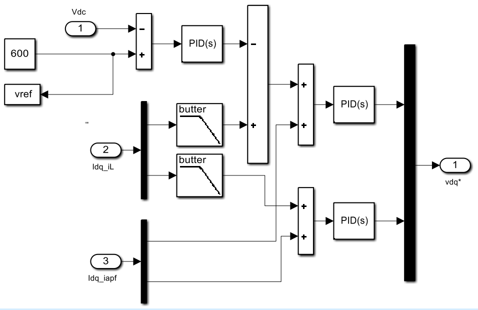
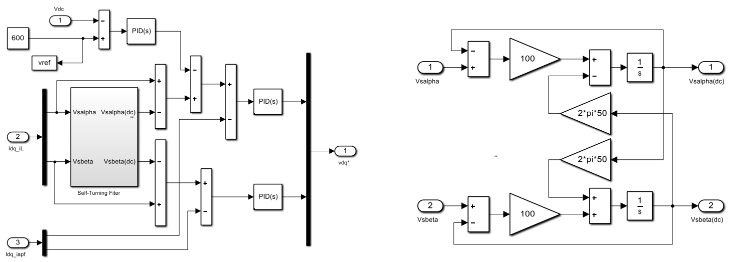


Fig. 9 (a). Simulation model LPF based harmonic extraction.



(i) **(ii)**

Fig. 9 (b). Simulink model of STF based harmonic extraction.

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Table 1. Parameters of SAPF

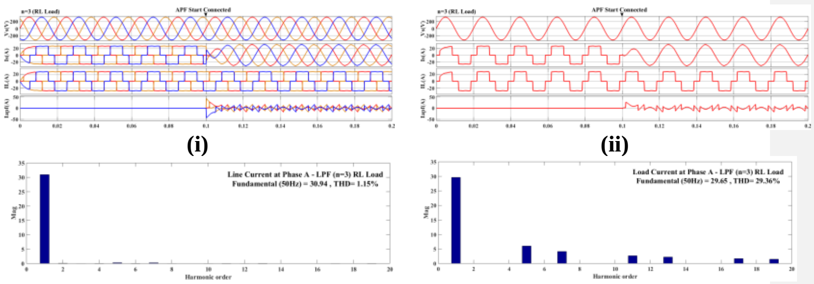
Parameter	***Value***
Voltage source	400 Vrms 50 Hz
Smoothing Inductor, I_{apf}	5 mH
Capacitor Link, C_{dc}	3300 µF 400V (each)
Line Inductor, I_l	2 mH
Switching frequency	20 kHz
Resistive Load	Rectifier + 20 Ω
Inductive Load	Rectifier + 50 mH (Series with 20 Ω)
Capacitive Load	Rectifier + 100 µF (Parallel with 20 Ω)

The voltage supply for this experiment is using balanced sinusoidal source voltage as stated in expression below.

$$V_{an} = 326 \sin 100\pi t \tag{34}$$

$$V_{bn} = 326 \sin(100\pi t - 120°) \tag{35}$$

$$V_{cn} = 326 \sin(100\pi t + 120°) \tag{36}$$



(i) **(ii)** **(iii)** **(iv)**

Fig. 10. LPF based harmonic extraction for inductive load at *n*=3: (i) three-phase line voltage, three-phase line current, three-phase load current and three-phase APF current, (ii) voltage and current at Phase A, (iii) THD of line current at Phase A and (iv) THD of load current at Phase A.

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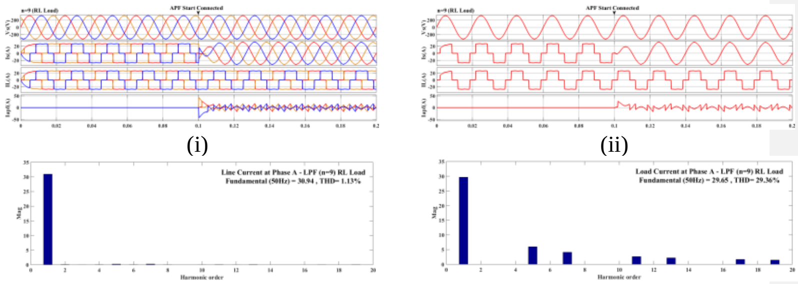

(i) (ii) (iii) (iv)

Fig. 11. LPF based harmonic extraction for inductive load at *n* = 9: (i) three-phase line voltage, three-phase line current, three-phase load current and three-phase APF current, (ii) voltage and current at Phase A, (iii) THD of line current at Phase A (iv) THD of load current at Phase A.

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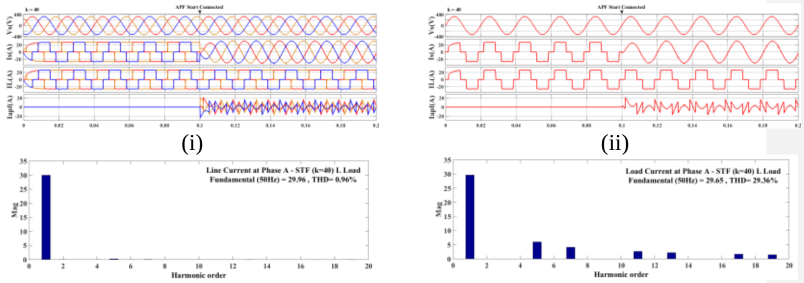
Fig. 10 and Fig. 11 show the results obtained according to LPF based harmonic extraction method for inductive load at filter order *n* of 3 and 9. Based on the results, THD for *n* = 3 reduces from 29.36% (load current) to 1.15% (line current). Meanwhile, for *n* = 9, the THD drops form 29.36% (line current) to 1.13% (line current). The highest number of *n* will perform better mitigation of harmonics due to load current.



(i) (ii)

(iii) (iv)

Fig. 12. STF based harmonic extraction for inductive load at *K*=40: (i) three-phase line voltage, three-phase line current, three-phase load current and three-phase APF current, (ii) voltage and current at Phase A, (iii) THD of line current at Phase A and (iv) THD of load current at Phase A.

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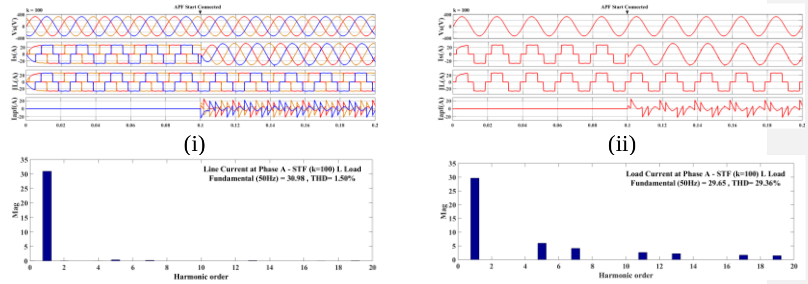

(i) (ii)

(iii) (iv)

Fig.13. STF harmonic extraction for Inductive load at *K*=100: (i) three-phase line voltage, three-phase line current, three-phase load current and three-phase APF current, (ii) voltage and current at Phase A, (iii) THD of line current at Phase A and (iv) THD of load current at Phase A.

Commented [WU18]: 18.Revise Fig 13i, Fig 13ii, Fig 13iii, and Fig 13iv into four table rows (not two columns).

Fig. 12 and Fig. 13 show the results obtained according to STF based harmonic extraction method for inductive load at selective parameter *K* 40 and 100. Based on the results, THD for *K*=40 reduces from 29.36% (load current) to 0.96% (line current). Meanwhile, for *K*=100 the THD drops from 29.36% (load current) to 1.50% (line current). The lowest number of *K* will perform better mitigation of harmonics due to the load current.

In additional, both of LPF and STF based harmonic extraction methods are tested with several of load, *n* for LPF and *K* for STF. The summarized performance of both algorithms are tabulated in Table 2 and Table 3 respectively. From Table 2, the increased value of *n* in LPF will produce better percentage of THD of line current for all tested loads. Meanwhile for Table 3, the decreased value of *K* in STF will produce better percentage of THD of line current for all tested loads.

Table 2. Performance of LPF with several loads

Load	LPF (THD of line and load current)														
	n = 1			n = 3			n = 5			n = 7			n = 9		
	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%
Resistive	29.47	3.98	86.5	29.47	1.53	94.8	29.47	1.50	94.9	29.47	1.50	94.9	29.47	1.50	94.9
Inductive	29.36	4.07	86.1	29.36	1.15	96.1	29.36	1.14	96.1	29.36	1.13	96.2	29.36	1.13	96.2
Capacitive	55.01	4.37	92.1	55.01	3.11	94.3	55.01	3.05	94.5	55.01	3.05	94.5	55.01	3.05	94.5

Table 3. Performance of STF with several loads

Load	STF algorithm technique (THD of line and load current)														
	K = 20			K = 40			K = 60			K = 80			K = 100		
	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%	Load (%)	Line (%)	Δ%
Resistive	29.47	1.34	95.5	29.47	1.36	95.4	29.47	1.45	95.1	29.47	1.58	94.6	29.47	1.75	94.1
Inductive	29.36	0.93	96.8	29.36	0.96	96.7	29.36	1.09	96.3	29.36	1.29	95.6	29.36	1.5	94.9
Capacitive	32.51	1.59	95.1	32.51	1.72	94.7	32.51	1.87	94.2	32.51	2.05	93.7	32.51	2.25	93.1

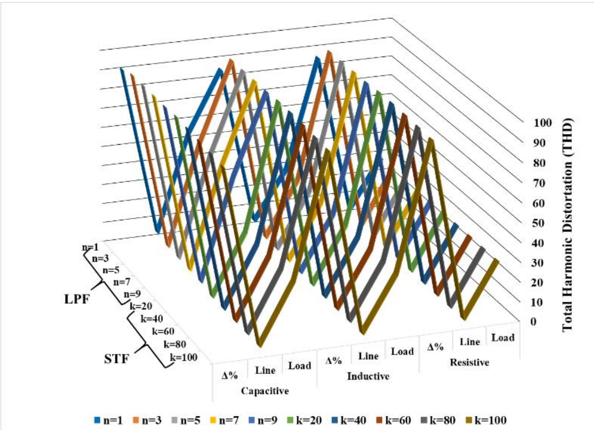

Fig. 14. Percentage reduction of THD of current for LPF and STF algorithms

Commented [WU19]: 19. Revise Figure 14 into a 3-axis bar graph to explain the value of THD increase according to the author's proposed model and then, explain the analysis in as much detail as possible.

Fig. 14 shows the percentage reduction of THD of line current for both LPF and STF algorithms. Both algorithms are capable to mitigate more than 85% of THD of load current. The high value of order in LPF contributes less value of THD, due to that the higher order will produce frequency response approaching to the ideal frequency response of LPF as shown early in Figure 4. In other words, the effect of higher order will shift the roll-off frequency response near to the ideal shape of LPF with angle perpendicular to 90º. However, the high order may cause the equation become more complex which contributes to increment of calculation time in the processor.

5. Conclusion

This paper demonstrates the performances of LPF and STF based harmonic extraction algorithms in CHB MLI SAPF. To obtain better percentage of THD of line current, the filter's order needs to be increased in LPF based harmonic extractions; meanwhile, the value of selective parameter needs to be decreased in STF based harmonic extraction. Based on the simulation results, both harmonic extractions have successfully operated CHB MLI SAPF with THD to be below 5%, as to follow the IEEE 519 Standard. STF based harmonic extraction is capable of mitigate more THD in load current compare to LPF based harmonic extraction. To achieve same performance as STF, the LPF needs to perform with high-order complex mathematical equations that contribute to creating time delay and at the same time, decreasing performance of SAPF. Implementing high order of LPF based harmonic extraction in hardware development is even more difficult.

Commented [WU20]: 20.Describe in detail the weaknesses of your method and the future work needed to improve these weaknesses. Explain in a last single paragraph in the conclusion section.

References

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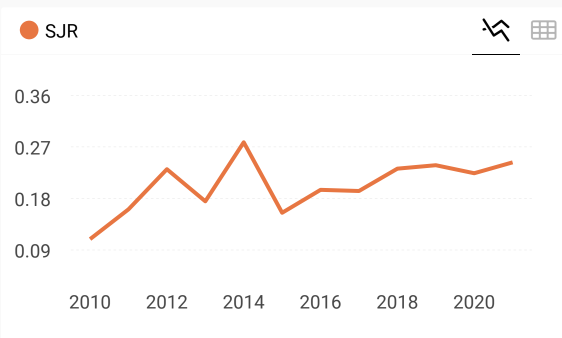

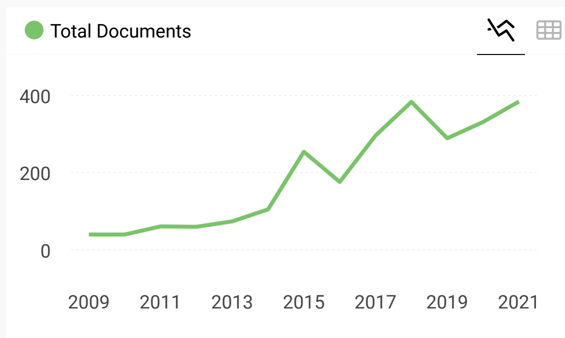

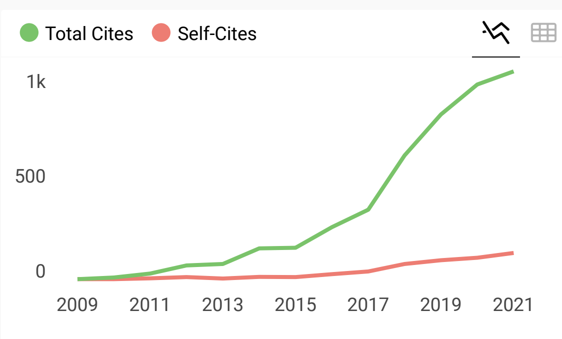

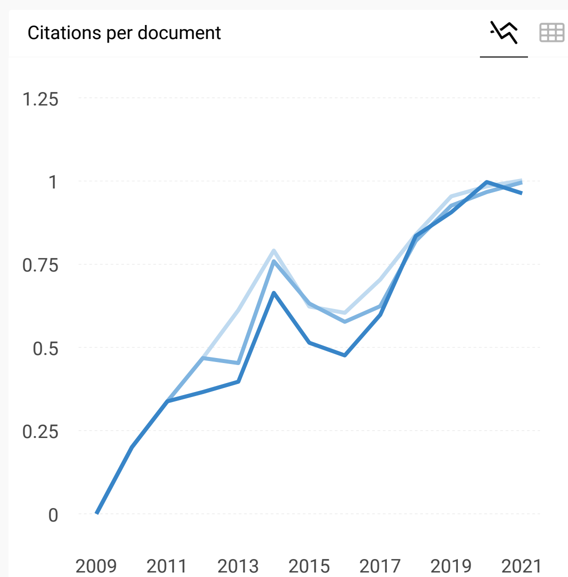

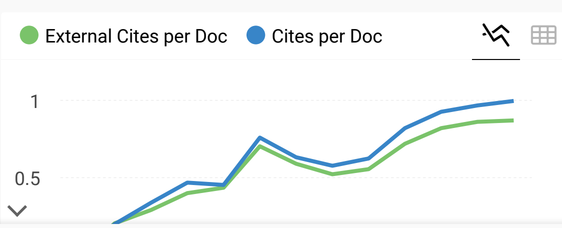

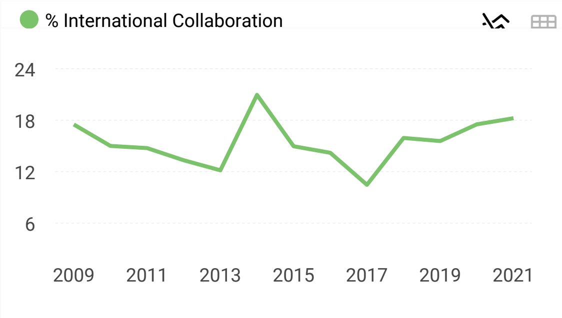

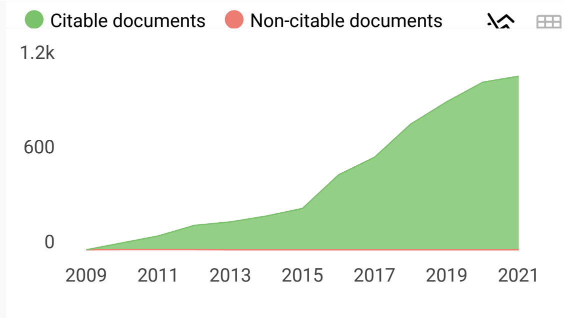

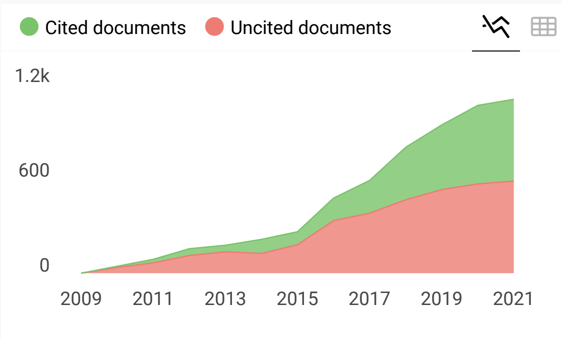

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Thank you

Sudhakiran Gunda 2 years ago

Could you please tell me the duration for this entire process.
I would like to know the time taken for publication.

Thankyou

SCImago Team

Melanie Ortiz 3 years ago

Dear Supreetha, thanks for your participation! Best Regards, SCImago Team

K

Khaled 3 years ago

Hello there!
I have a little question about the publication process timeline, Can i know please how long will take between sending an article and (journal answer by acceptance/rejection) and finally the paper's online availability ????

K

Khaled 3 years ago

Thanks alot for your valuable response
Are there any publication fees or not ???????

A

Ali 3 years ago

Dear khaled
The timeline for publishing in this journal about 2-3 months for final acceptance and may be 9 months for online publication
with my regards

SCImago Team

Melanie Ortiz 3 years ago

Dear Ali, thanks for your participation! Best Regards, SCImago Team

SCImago Team

Melanie Ortiz 3 years ago

Dear Khaled,
thank you for contacting us.
Sorry to tell you that SCImago Journal & Country Rank is not a journal. SJR is a portal with scientometric indicators of journals indexed in Elsevier/Scopus.
Unfortunately, we cannot help you with your request, we suggest you to visit the journal's homepage or contact the journal's editorial staff , so they could inform you more deeply.
You can see the updated journal's information just above .
Best Regards, SCImago Team

A

ASWANT KUMAR SHARMA 3 years ago

I have published a paper with JESTEC in a proper time line. It is good if JESTEC provide DOI for article published with them

reply

M

Malathi Kunnudaiyan 2 years ago

Have paid any fees for the publication sir?

R

rati saluja 3 years ago

The journal that provides best services, never a single follow up query left unaswered. I had written several research papers in numerous journals, but I feel pride the way "Journal of Engineering Science and Technology" works, they reviwed eveery mm of my manuscript. Their editing team is soul of the body. Mr. Obaidi shares every detail regaring the review process as well as time duration, that made the process easy. Publishing in a reputed journal takes time, So eagerly waiting for the same.
Thanks a million to Dr. Abdulkareem Sh. Mahdi Al-Obaidi for sharing a wonderful platform to enhance one'knowledge and research.

Hats off

A happy author

reply

M

Melva Silitonga 4 years ago

This journal template has been used for the 2019 Kyoto APLSBE template that I have participated in, I am interested in the content of this journal and wish for publication in this journal

reply

W

Wajde Alyhya 4 years ago

Hi
I sent a manuscript for publication in this journal and I received two months later seven reviewers' comments. I answered all their comments, however, I have not received an acceptance or rejection letter till now. I sent more than one emails regarding the status of my manuscript without an answer. I do not know what to do after nearly more than 6 months of waiting.

reply

A

Abdulkareem Sh. Mahdi Al-Obaidi 3 years ago

Dear Wajde
We thank you for the comment.
As you mentioned your experience with JESTEC, i wonder why you did not mention that your paper is accepted and will be published soon.
It is good to give negative feedback for improvment, we thank you but it is also fair to tell positive feedback, right?

E

Emmanuel 4 years ago

@ Elena:I humbly suggest that the web link of all journals should be published alongside their name.This will eliminate the faking of journals in your data base.

reply

W

Wajde Alyhya 4 years ago

Dear All
Could you please tell me how long it takes to be accepted and published online.
Thanks

reply

D

Dr. mohammed alwazzan 4 years ago

3 to 4 month

Elena Corera 4 years ago SCImago Team

Dear Wadje, in the link below you will find the information corresponding to the author's instructions of this journal. Best regards, SCImago Team
http://jestec.taylors.edu.my/instructions.html

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