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UNIVERSITAS BHAYANGKARA SURABAYA
LEMBAGA PENELITIAN DAN PENGABDIAN PADA MASYARAKAT
(LPPM)
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SURAT KETERANGAN

Nomor: Sket/44/I/2023/LPPM/UBHARA

Kepala Lembaga Penelitian dan Pengabdian kepada Masyarakat (LPPM) Universitas Bhayangkara Surabaya menerangkan bahwa:

Nama : Dr. Amirullah, ST, MT.
NIP : 197705202005011001
NIDN : 0020057701
Unit Kerja : Universitas Bhayangkara Surabaya

Benar telah melakukan kegiatan:

1. Mereview makalah jurnal internasional bereputasi berjudul "Development of Fast-Transient Response DC-DC Converter with Low Output-Voltage Ripple" dari Journal of ICT Research and Applications (JICTRA), Publisher: Institut Teknologi Bandung (ITB) Tahun 2020, Terindeks Scopus Q3.
2. Telah melakukan korespondensi email dengan editor/pengelola jurnal dalam rangka mereview substansi materi makalah jurnal dalam selang waktu yang telah ditentukan sebelumnya. Bukti korespondensi email dan bukti pendukung adalah benar sudah dilakukan oleh yang bersangkutan serta sudah dilampirkan bersama surat ini.

Demikian surat keterangan ini dibuat untuk kepentingan kelengkapan pengusulan Guru Besar.

Surabaya, 20 Januari 2023
Kepala LPPM

Drs. Heru Irianto, M.Si.
NIP. 9000028

Lampiran 1

Bukti Korespondensi Email dengan Editor/Pengelola Jurnal

Ubhara Surabaya

Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

[jictra] Able to Review

1 pesan

Amirullah Amirullah <amirullah14@mhs.ee.its.ac.id> 11 Oktober 2020 pukul 06.52
Kepada: Journal of ICT Research and Applications <jictra@lppm.itb.ac.id>
Cc: amirullah@ubhara.ac.id

Journal of ICT Research and Applications:

I am able and willing to review the submission, "Development of Fast-Transient Response DC-DC Converter with Low Output-Voltage Ripple," for Journal of ICT Research and Applications. Thank you for thinking of me, and I plan to have the review completed by its due date, 2020-10-14, if not before.

Amirullah Amirullah

Journal of ICT Research and Applications
http://journals.itb.ac.id/index.php/jictra

Ubhara Surabaya

Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Re: 14138 [jictra] Article Review Request from Journal of ICT Research and Applications

2 pesan

AMIRULLAH ITS <amirullah14@mhs.ee.its.ac.id> 11 Oktober 2020 pukul 06.49
Kepada: jictra@lppm.itb.ac.id
Bcc: amirullah@ubhara.ac.id

Dear Dr. Achmad Munir,

I apologize to you because just read this email. If you give time I would like to review this paper depend on your request.

For this reason, I need to help you to send me a username and password.

Dr. Amirullah
Electrical Engineering
Universitas Bhayangkara Surabaya
Power Quality, Power Electronics, and Renewable Energy Research
081949649423

On Wed, Sep 23, 2020 at 10:33 AM <jictra@lppm.itb.ac.id> wrote:

> Dear Amirullah Amirullah,
>
> Because of your substantial expertise related to the manuscript, "Development of Fast-Transient Response DC-DC Converter with Low Output-Voltage Ripple," I would like to ask your assistance in determining whether the above-mentioned manuscript is appropriate for publication in Journal of ICT Research and Applications. External reviews are the single most important element in critically evaluating a manuscript and we almost invariably follow the advice of the Reviewers. We particularly value the identification of routine work unlikely to be of interest to the community, in order to prevent its publication in the Journal. The submission's abstract is inserted below, and I hope that you will consider undertaking this important task for us.
>
> Please log into the journal web site by 2020-09-30 to indicate whether you will undertake the review or not, as well as to access the submission and to record your review and recommendation. The web site is http://journals.itb.ac.id/index.php/jictra
>
> The review itself is due 2020-10-14.
>
> Submission URL: http://journals.itb.ac.id/index.php/jictra/reviewer/submission/30521?key=ACCESS_KEY
>
> If you does not know or forget the password for the journal's web site, you can use this link to reset your password (which will then be emailed to you along with your username): http://journals.itb.ac.id/index.php/jictra/login/lostPassword
>
> If you are unable to review this manuscript, we would appreciate your suggestions of alternate reviewers (contact information would be helpful).
>
> Thank you for considering this request.
>
> Sincerely,

Dr. Achmad Munir
Journal of ICT Research and Applications
jictra@lppm.itb.ac.id

AMIRULLAH ITS <amirullah14@mhs.ee.its.ac.id> 11 Oktober 2020 pukul 08.35
Kepada: jictra@lppm.itb.ac.id
Cc: AMIRULLAH ITS <amirullah14@mhs.ee.its.ac.id>
Bcc: amirullah@ubhara.ac.id

Dear Dr. Achmad Munir,

I just have reviewed the paper in Journal of ICT Research and Applications LPPM ITM.

The title is **Development of Fast-Transient Response DC-DC Converter with Low Output-Voltage Ripple.**

from my account in link: http://journals.itb.ac.id/index.php/jictra/user.

Dr. Amirullah
Universitas Bhayangkara Surabaya
[Kutipan teks disembunyikan]

Ubhara Surabaya

Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

Re: [jictra] Article Review Acknowledgement from Journal of ICT Research and Applications

1 pesan

AMIRULLAH ITS <amirullah14@mhs.ee.its.ac.id> 13 Oktober 2020 pukul 18.30
Kepada: Journal of ICT Research and Applications <jictra@lppm.itb.ac.id>
Bcc: amirullah@ubhara.ac.id

Dear Dr.Eng. Achmad Munir, ST,M.Eng.
Editor in Chief Journal of ICT Research and Applications

Thanks a lot for your email.

However, is there any certificate of appreciation for me from LPPM ITB for reviewing this paper?

Because it has a credit value for me in order to achieve Lektor Kepala/Professor in the next time.

Thanks a lot for your response.

Dr. Amirullah
Power Quality, Power Electronics, and Renewable Energy Research
Universitas Bhayangkara Surabaya

On Mon, Oct 12, 2020 at 8:23 PM Journal of ICT Research and Applications <jictra@lppm.itb.ac.id> wrote:

> Dear Amirullah Amirullah,
>
> This is to confirm that we have received your review for the manuscript, "Development of Fast-Transient Response DC-DC Converter with Low Output-Voltage Ripple," for Journal of ICT Research and Applications. We appreciate the time that you have contributed to this important component of the peer review process.
>
> Your cooperation is greatly appreciated, and we hope that you will consider the Journal of ICT Research and Applications as a potential journal for your own next publication.
>
> Kind regards,
>
> Dr.Eng. Achmad Munir, ST,M.Eng.
> Journal of ICT Research and Applications
> jictra@lppm.itb.ac.id
>
> ---
> Journal of ICT Research and Applications
> http://journals.itb.ac.id/index.php/jictra

Amirullah Ubhara Surabaya <amirullah@ubhara.ac.id>

[jictra] Article Review Completed

1 pesan

Amirullah Amirullah <amirullah14@mhs.ee.its.ac.id> 21 November 2020 pukul 06.19
Kepada: ournal of ICT Research and Applications <jictra@lppm.itb.ac.id>
Cc: Journal of ICT Research and Applications <jictra@lppm.itb.ac.id>

Journal of ICT Research and Applications:

I have now completed my review of "Development of Fast-Transient Response DC-DC Converter with Low Output-Voltage Ripple" for Journal of ICT Research and Applications, and submitted my recommendation, "Accept Submission."

Amirullah Amirullah

Journal of ICT Research and Applications
http://journals.itb.ac.id/index.php/jictra

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108K

Lampiran 2

Bukti Pendukung

A Novel Boost-Buck Converter Architecture for Improving Transient Response and Output-Voltage Ripple

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Abstract. Buck-boost converter architecture is widely used in the development of DC-DC converter. Many techniques and algorithms have been introduced to improve the transient response of buck-boost converter. However, due to the opposite trend between the output current and voltage changes, the undershoot or overshoot in the output voltage is still apparent inevitably. In order to overcome this problem, a novel architecture of boost-buck converter is proposed to build fast-transient response DC-DC converter. The converter consists of a cascaded configuration of the boost and buck stages. The boost-stage converts input voltage into shared capacitor voltage, and the buck-stage supplies energy to the load by converting the shared capacitor voltage into output voltage. By harnessing the energy stored in the shared capacitor, the transient response of the boost-buck architecture can be improved to 2 μs in a step-up load current change of 1 A with an output-voltage ripple of 15 mV.

Keywords: *DC-DC Converter, Boost, Buck, Fast-transient, Low-ripple.*

1 Introduction

DC-DC converter has been widely used in power management technology for the development of modern integrated circuits and systems. The widespread use of portable devices (e.g. digital camera, cellular phone, and tablet personal computer) requires high-performance DC–DC converter for ensuring the quality of power supply. In battery powered systems, a fully charged battery usually possesses higher-than-nominal voltage, while the discharged battery has the lower one. In order to generate a stable power supply voltage, a buck-boost

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converter is generally used due to its wider input voltage range [1]-[3]. Moreover, the stable voltage is required in the high-performance systems to cope with the dynamically varying workload especially in modern microprocessor systems. When the system switches between idle mode and active mode, there exists a large amount of difference in the required current loads. In the meantime, in active mode, the processor usually has varying loads. Unfortunately, the output current slew rate limitation of the buck-boost converter is usually restricted by its inductor. Thus, the supply voltage fed by the converter will encounter undershoot or overshoot and deviate from its nominal value. The overshoot may cause higher chip temperature, while the undershoot inducing too low supply voltage may force the processor to insert "idle" instructions for reducing load current. Furthermore, the processor may fail to execute any instructions or dismiss some data [4]-[5]. The aforementioned facts show that the slew rate limitation in output current must be mitigated, and fast-transient response becomes an important design consideration in the DC-DC converter.

In the buck-boost converter, incapability of the inductor to suddenly change the current will violate the output voltage. This consequently takes some times to return the output voltage into its nominal value, and yields undershoot or overshoot in the output voltage. Furthermore, when the converter works in boost-mode, it suffers from output current change due to the opposite trend between output-current and output-voltage changes.

Several methods and algorithms have been developed to alleviate the undershoot or overshoot in the output voltage of buck-boost converters [6]-[12]. In Ref. [6], adaptive pulse skipping and adaptive compensation capacitance techniques have been used to reduce the transient response to 59 μs in a 400 mA load. A converter is reported to be able to achieve a fastest transient response in

45 μs, under a load current of 200 mA, using a hybrid buck–boost feedforward technique [7]. In general, the transient response can be reduced by using higher switching frequency. Using a switching frequency higher than 1 MHz may reduce the transient response below 20 μs [8]-[12]. In Ref. [8], a switching frequency of 3 MHz can support an on-duty modulation to achieve a fast line transient response of 17.2 μs at the load change from 10 to 600 mA. Meanwhile, in Ref. [11], by utilizing a load dependent on/off time, the transient response can be improved into 10 μs at a 600 mA load current. Utilization of a higher switching frequency may improve the transient response, yet produces higher switching loss and circuit diagram complexity. The aforementioned studies in Refs. [8]-[12] may enhance the quality of transient response, albeit the shoot in the output voltage is still inevitable. This fact brings the development of a new method for fast-transient response DC-DC converter is of interest.

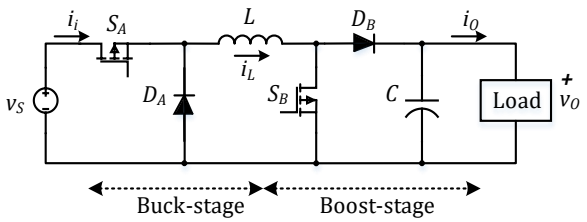
In this paper, a novel cascaded architecture of boost-buck converter is proposed. Similar architecture had been developed for Wireless Power Transfer System [13] and electric bus charger [14]. In Ref. [13], the architecture is used to perform an optimal impedance matching and dynamic load isolation. Meanwhile, the architecture given in Ref. [14] is utilized to accommodate input and battery voltage. Both applications are not intended to improve the transient response.

In this study, the boost-buck architecture for improving transient response is investigated. This manuscript is divided into four sections. Section 1 presents the background and overview of the proposed method. In Section 2, the architecture description and theoretical formulation of the new method as well as the working operation principal of the proposed converter are discussed. Several important cases are simulated in Section 3. The experimental results are subsequently analyzed and compared with those obtained by similar

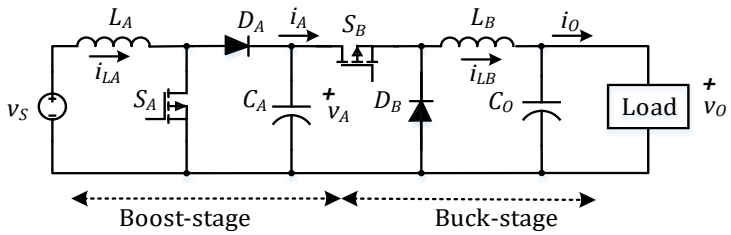
experiments on conventional buck-boost converters. Finally, conclusions are drawn in Section 4.

2 Research Method

Figure 1(a) shows a buck-boost converter widely used while Figure 1(b) shows the proposed boost-buck converter. They have a lower voltage stress of the components due to non-inverting output voltage [15]-[17]. The proposed boost-buck converter is a development of the previous one [18]. It uses separate inductors for boost and buck stages. An additional shared capacitor C_A filters the boost-stage output voltage and constitutes a voltage source for the buck-stage.



(a) a non-inverting buck-boost converter



(b) the proposed boost-buck converter

Figure 1 A non-inverting buck-boost converter and the proposed boost-buck converter

2.1 The boost-stage

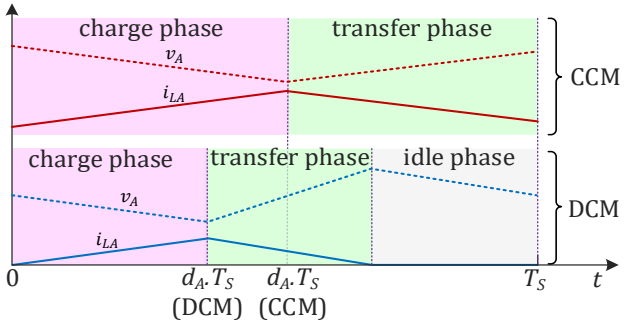
In the proposed boost-buck converter, the boost-stage steps up the input voltage v_s to the shared capacitor voltage v_A. Figure 2(a) shows the key waveform when the boost-stage operates in discontinuous-current mode (DCM) and

continuous-current mode (CCM) with switching period T_S and duty cycle d_A. When the stage works in DCM, three unique phases appear in each switching period: charge, transfer, and idle phases [11]. During the charge phase, the power switch S_A is on, thus the voltage source v_S energizes the boost-inductor L_A while the buck-stage is supplied by the energy stored in the shared capacitor. Meanwhile, in the transfer phase, the power switch S_A is turned off and stored energy in the boost-inductor is released and becomes a boost-stage output current i_A. When the stored energy in the boost-inductor has run out, the stage falls into idle phase. By applying the KVL and KCL, the state space representation for charge phase can be expressed as follows

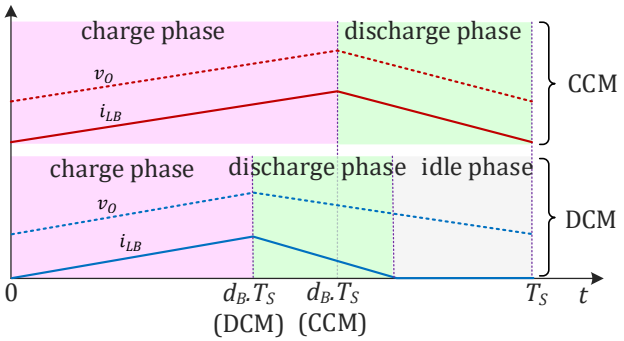
$$\begin{bmatrix} \frac{di_{LA}(t)}{dt} \\ \frac{dv_A(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{C_A R_L} \end{bmatrix} \begin{bmatrix} i_{LA}(t) \\ v_A(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_A} \\ 0 \end{bmatrix} v_S \tag{1}$$

Meanwhile, the state space representation for transfer and idle phase can be stated as follows

$$\begin{bmatrix} \frac{di_{LA}(t)}{dt} \\ \frac{dv_A(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_A} \\ \frac{1}{C_A} & -\frac{1}{C_A R_L} \end{bmatrix} \begin{bmatrix} i_{LA}(t) \\ v_A(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_A} \\ 0 \end{bmatrix} v_S \tag{2}$$



(a) boost-stage



(b) buck-stage

Figure 2 Key waveform of the boost and buck stages

When there is no net change in output current and voltage during a switching period, the stage reaches steady-state. From the Eqs. (1) – (2), the output current i_A in DCM can be expressed as

$$i_A = \frac{{v_S}^2 {d_A}^2 T_S}{2(v_A - v_S)L_A} \tag{3}$$

Therefore, the boost-stage duty cycle d_A may track the boost-stage output current i_A as

$$d_A = \sqrt{\frac{2i_A(v_A - v_S)L_A}{{v_S}^2 T_S}} \tag{4}$$

When the stage works in CCM, only two unique phases appear: charge and transfer phases. The changes of output current Δi_A and output voltage Δv_A within one switching period T_S can be derived as

$$\Delta i_A = \frac{T_S}{L_A}(v_S - v_A + d_A v_A) \tag{5}$$

$$\Delta v_A = \frac{T_S}{C_A}(i_{LA}(1 - d_A) - i_A) \tag{6}$$

The stage reacts to output current change i_A by determining a new duty cycle d_A in order to change i_{LA}.

$$d_A = \frac{\Delta i_A v_A L_A + (v_A - v_S) v_S T_S}{v_S v_A T_S} \tag{7}$$

The output current condition where the boost-stage is at the boundary between DCM and CCM is

$$i_{O(D/C)} = \frac{(v_A - v_S) {v_S}^2 T_S}{2 {v_A}^2 L_A} \tag{8}$$

The relationship between the changes of the output current Δi_A and voltage Δv_A can be deducted as

$$\Delta v_A = -\frac{\Delta i_A i_A v_A L_A}{{v_S}^2 C_A} \tag{9}$$

Eq. (9) clearly stated an opposite trend between both parameters. This essential problem implies that the output current increases cause the output voltage drops and vice versa. This induces output voltage violation in a buck-boost converter due to the stage directly supplies energy to the load. Therefore, the stability of the output voltage suffers from the output current change when a buck-boost converter works in boost-mode. Although it is possible to alleviate this problem, it will be still inevitable in a transient period and produce an overshoot or undershoot in the output voltage.

2.2 The Buck-stage

The buck-stage steps down the shared capacitor voltage v_A to the output voltage v_O. Figure 2(b) shows the key waveform when the buck-stage operates in DCM and CCM with switching period T_S and duty cycle d_B. When the stage works in DCM, three unique phases appear in each switching period: charge, discharge, and idle phases [11]. During the charge phase, the power switch S_B is on, thus,

the voltage source v_S energizes the inductor L_B. Meanwhile during the discharge phase, the power switch S_B is turned off and energy stored in the buck-inductor is released to the output capacitor and supply the load. When there is no more energy stored in the buck-inductor, the stage falls into idle phase. By applying the KVL and KCL, a state space representation for charge phase can be expressed as follows

$$\begin{bmatrix} \frac{di_{LB}(t)}{dt} \\ \frac{dv_O(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_B} \\ \frac{1}{C_O} & -\frac{1}{C_O R_L} \end{bmatrix} \begin{bmatrix} i_{LB}(t) \\ v_O(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_B} \\ 0 \end{bmatrix} v_A \tag{10}$$

Meanwhile, the state space representation for discharge and idle phase can be stated as

$$\begin{bmatrix} \frac{di_{LB}(t)}{dt} \\ \frac{dv_O(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_B} \\ \frac{1}{C_O} & -\frac{1}{C_O R_L} \end{bmatrix} \begin{bmatrix} i_{LB}(t) \\ v_O(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_A \tag{11}$$

When the stage reaches steady-state, the output current in DCM can be calculated as

$$i_O = \frac{v_A - v_O}{2L_B} {d_B}^2 T_S \left(1 + \frac{v_A - v_O}{v_O}\right) \tag{12}$$

Therefore, the buck-stage duty cycle d_B may track the output current i_O as follow

$$d_B = \sqrt{\frac{2 i_O L_B v_O}{v_A (v_A - v_O) T_S}} \tag{13}$$

Meanwhile, when the stage works in CCM, only two unique phases appear: charge and discharge phases. By using Eqs. (10) and (11), the changes of buck-

inductor current Δi_{LB} and output voltage Δv_O within one switching period T_S can be derived as Eqs. (14) and (15) respectively.

$$\Delta i_{LB} = \frac{T_S}{L_B}(v_A d_B - v_O) \tag{14}$$

$$\Delta v_O = \frac{T_S}{C_O}(i_{LB} - i_O) \tag{15}$$

In this mode, the stage reacts to output current changes Δi_O by determining a new duty cycle in order to change i_{LB}. From the Eq. (14), the duty cycle d_B can be calculated as

$$d_B = \frac{\Delta i_O L_B + v_O T_S}{T_S v_A} \tag{16}$$

The output current condition where the buck-stage is at the boundary between DCM and CCM is

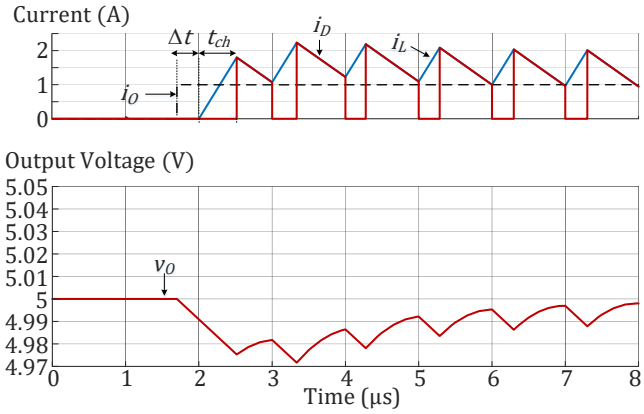
$$i_{O(D/C)} = \frac{v_A v_O - {v_O}^2}{2 L_B v_A} T_S \tag{17}$$

2.3 The Operational Principal of The Boost-Buck Converter

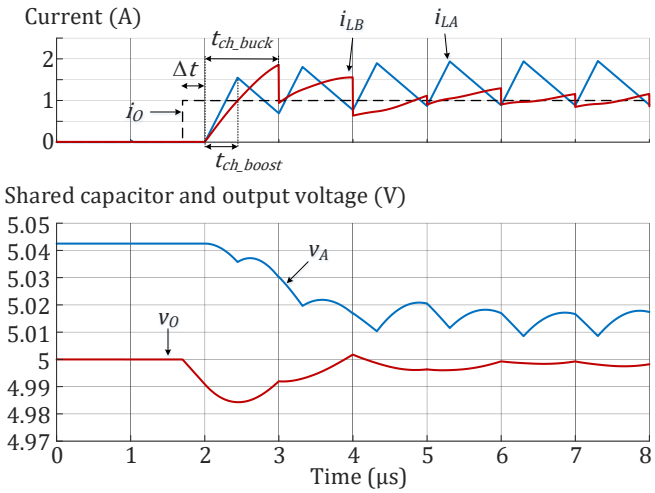
The stability of the output voltage in a buck-boost converter suffers from the output current change when it works in CCM of boost-mode. The upper part of Figure 3(a) shows an example for waveforms of the inductor current i_L (blue line) and diode current i_D (red) and load current i_O (black-dashed). As a load current of 1 A is applied in t = 1.7 μs, the boost-stage reacts by increasing its duty cycle to prolong the charge phase in order to increase the inductor current. However, during this phase, there is no energy transferred from the inductor to the load. This causes voltage drop in transient period, $\Delta t + t_{ch}$. The deleterious effect of output current change is clearly illustrated in an output voltage curve in the lower part of Figure 3(a).

A simplified, qualitative way to visualize the basic different operation of the proposed boost-buck converter and the conventional buck-boost converter is to consider the use of shared capacitor as a temporary energy stored element. The energy stored in the shared capacitor can be used to maintain the output voltage to be the nominal value if its voltage v_A is higher than the output voltage v_O. Such energy can be defined as $E_A = \frac{1}{2} C_A({v_A}^2 - {v_O}^2)$, so that, the shared capacitor voltage must be available when the converter will be drawn by a load current of i_O can be derived as follow,

$$v_A = \sqrt{\frac{2(i_{O(max)} - i_O) v_O {v_S}^2 T_S + 2(i_{O(max)} - i_O)^2 {v_O}^2 L_A}{C_A {v_S}^2} + {v_O}^2} \tag{18}$$



(a) in buck-boost converter



(b) in boost-buck converter

Figure 3 Simulated current and voltage when load current is applied

The actual shared capacitor voltage may not equal to v_A as calculated in Eq. (18). On forgoing analysis, v_{A_ref} defines the result of Eq. (18) and v_A is the actual shared capacitor voltage. For recovering the energy balance after output current changes, a PID compensation is adopted to return v_A back to v_{Aref} by slightly increasing or decreasing the duty cycle for a period of time.

3 Results and Discussions

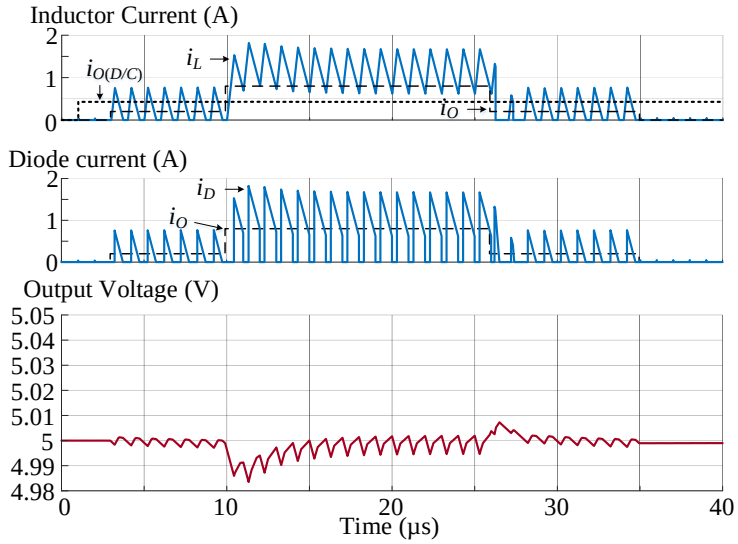
The proposed boost-buck DC-DC converter is designed to achieve a faster transient response with smaller output-voltage ripple. Several simulations utilizing system parameters listed in Table 1 are conducted to investigate the performance of the proposed converter. For sake of the verification of the obtained transient response, load current changes are applied to the converter in a short period.

Tabel 1 Parameters of proposed boost-buck converter

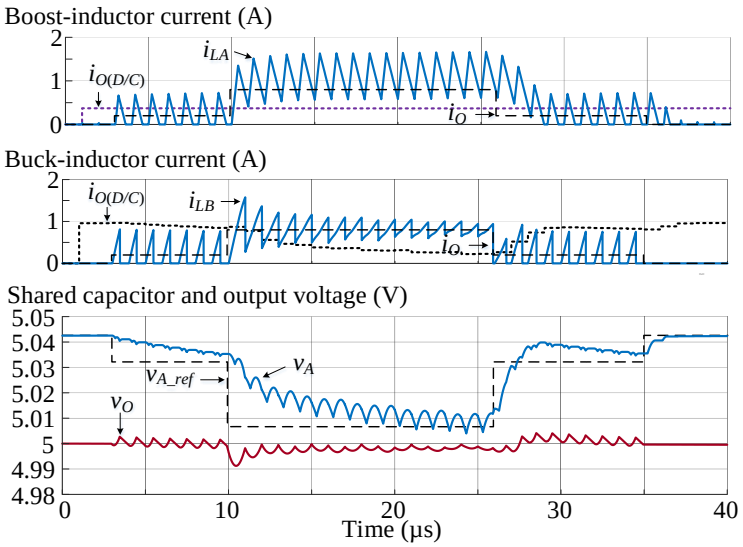
Parameters	Symbols	Values
Input voltage	v_S	3.5 V
Output voltage	v_O	5 V
Boost-inductance	L_A	1 µH
Buck-inductance	L_B	22 nH
Shared capacitor	C_A	33 µF
Output capacitor	C_O	33 µF
Maximum output current	i_O(max))	1 A
Switching frequency	f_S	1 MHz

Figure 4 presents the comparison of simulated transient waveform for current and voltage between a buck-boost converter and proposed boost-buck converter. In this simulation, an initial step-up load current of 0.2 A is applied at t = 2.8 µs. Owing to the fact that i_O is lower than $i_{O(D/C)}$, the operation mode is set to DCM and new duty cycle is determined. In the proposed boost-buck one, the increased duty cycle yields the increase of boost-inductor current i_{LA} and buck-inductor current i_{LB}. In regards to the output voltage, as stated in Eqs. (4) and (13), the duty cycle of boost and buck stages of both converters have the same trends to their output voltages, therefore the shoot does not exist.

When a 0.6 A load change is applied at t = 9.8 µs, i_O is higher than $i_{O(D/C)}$. Thus, the converter increases the duty cycle and switches the operation mode to CCM. In a buck-boost converter, the increase of boost-stage duty cycle introduces the output voltage drop. Contrary, in the proposed converter, the increase of the boost-stage duty cycle results in the decrease of the shared capacitor voltage v_A only. In spite of this fact, as long as v_A is greater than v_O, the output voltage can be properly maintained constant by the buck-stage. By comparing the output current injected to the output capacitor, it can be seen that the diode current i_D in buck-boost converter is discontinuous or pulsating while the buck-inductor current i_{LB} in the proposed converter is a sawtooth. These phenomena induce the output-voltage ripple of the proposed converter is lower than that of the conventional buck-boost converter.



(a) in buck-boost converter



(b) in the proposed boost-buck converter

Figure 4 Simulated waveforms for current, voltage and duty cycle

As stated in Eq. (16), the duty cycle of the boost-state in CCM depends on the output-current change Δi_O and the DC level of the input voltage v_S and output voltage v_O. When the conventional buck-boost converter works in boost-mode,

the converter reacts to change the duty cycle according to Δi_O only because of the fixed values of v_S and v_O. Therefore, in case of a light-to-heavy load change, the duty cycle is raised for certain switching periods and returned back to the steady-state value afterwards. Meanwhile, in the proposed converter, the boost-stage determines the duty cycle according to the Δi_O and shared-capacitor voltage v_A. Due to the opposite reaction among both parameters, variation of the boost-stage duty cycle d_A in the proposed converter is smaller than that of the conventional converter. The similar trend also occurs to the boost-inductor current i_{LA}. This cause the boost-stage of the proposed converter seems to have a more sluggish response than that of the conventional one.

As the load goes lighter, the converter determines a lower duty cycle to decrease their inductor current. In buck-boost converter, a lower boost-stage duty cycle results in the decrease of charge phase while increasing transfer phase. More time for transfer phase increases the i_D and causes the upward violation in the output voltage. Meanwhile in the proposed converter, more time for transfer phase increases the boost-stage output current i_A and the shared capacitor voltage v_A. However, a decrease in output load current i_O will be followed by an increase in v_{A_ref} as in Eq. (18). Consequently, v_A will be able to reach v_{A_ref} faster.

In the proposed converter, when the output current changes, the buck-stage determines corresponding adjustment amount of the duty cycle according to Eqs. (13) or (16) to change the buck-inductor current in order to keep the output voltage constant at its nominal value. Due to the inductor's tendency to resist changes in current, the output current slew rate is fundamentally limited due to the presence of the buck-inductor. To allow more rapidly changes in the buck-inductor current, the buck-inductance may be reduced. This can be done due to the proposed architecture uses separate inductors for boost and buck stages.

Contrasting to the conventional buck-boost converter that use the same inductor for both stages, reducing the inductances may improve the transient response, but this will increase the output-voltage ripple when it works in boost-mode.

The buck-inductance must be carefully determined. Using a smaller buck-inductance will reduce $i_{O(D/C)}$, thus may force the buck-stage to work in DCM for more cases and increase the output-voltage ripple. The proposed converter uses a 22 nH buck-inductance. By harnessing the energy stored in the shared capacitor, the buck-stage allows the current to flow through the buck-inductor with a rate of change up to 1.91 A/μs when the maximum load current is applied from a no-load condition. Therefore, the stage is able to recover the output voltage in 2 μs. By comparing the transient response time and output-voltage ripple between buck-boost converter and the proposed converter in Figure 3 and Figure 4, it is clear that the transient response time of the boost-buck converter is shorter than that of a buck-boost one. Moreover, to further enhance the transient response and the efficiency, several methods have been introduced to develop the buck and boost converter may be developed in the proposed converter [19]-[22].

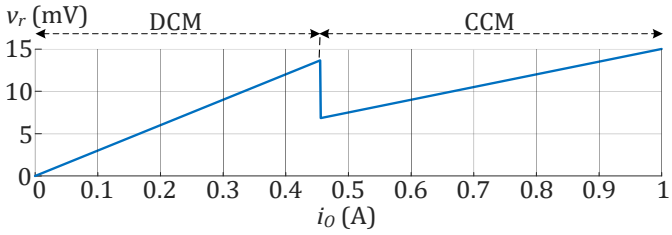


Figure 5 The output-voltage ripple as the output current

The proposed converter may perform a better output-voltage ripple v_r when drawn by a large output current and the buck-stage work in CCM. In this case, the buck-stage duty cycle d_B approaches one, thus C_A, L_B, and C_O constitute a

second order filter. Hence, the output-voltage ripple can be effectively diminished. Figure 5 exhibits the output-voltage ripple as the output current. The maximum value of output-voltage ripple is 13.6 mV when the buck-stage works in DCM and 15 mV when in CCM.

Table 2 Performance comparison of recent techniques developed in DC-DC converter

Technique	v_S and v_O	$i_{O(max)}$	f_S	$v_{r(max)}$	$t_{r(min)}$	L/C
Adaptive pulse skipping and compensation capacitance [6]	2.7~4.5 V 3 V	900 mA	1 MHz	N/A	59 µs @400 mA	2.2 µH/20 µF
Hybrid buck–boost feedforward [7]	2.7~4.5 V 3.3 V	500 mA	700 kHz	>200 mV	45 µs @200 mA	4.7 µH/47 µF
Direct path skipping and On-Duty Modulation [8]	3.0 V 2.8~5.5 V	1 A	3 MHz	88.3 mV	17.2 µs @600 mA	2.2 µH/33 µF
Hysteretic-current-mode [9]	2.5~5 V 3.3 V	400 mA	≤1.66 MHz	15 mV	15 µs @290 mA	1 µH/10 µF
Power-tracking with fast dynamic voltage scaling [10]	2.5~4.5 V 2~4 V	400 mA	5 MHz	>175 mV	15 µs @300 mA	1 µH/0.88 µF
Load-dependent on/off time [11]	3.3 V 1.8~5.0V	800 mA	3.3 MHz	90 mV	10 µs @600 mA	1.5 µH/10 µF
Pseudo-current Dynamic Acceleration [12]	3.3 V 1V~4.5V	200 mA	1 MHz	80 mV	2 µs @200 mA	22 µH/10 µF
Boost-buck architecture (Simulated in this work)	3.5~6 V 5 V	1 A	1 MHz	15 mV	2 µs @1 A	1+0.022 µH/ 33+33 µF

v_S/v_O = input/output voltage
$i_{O(max)}$ = maximum load current
f_S = switching frequency
$v_{r(max)}$ = maximum output-voltage ripple
$t_{r(min)}$ = minimum transient response time
L/C = capacitance and inductance used

Table 2 summarizes the measured characteristic of the published DC-DC converter. Using a 1 MHz switching frequency, a pseudo-current dynamic acceleration in Ref. [12] can be utilized to improve the transient response to 2 µs. However, the proposed boost-buck converter performs a better output voltage quality due to its lower output-voltage ripple. Therefore, the performance of the proposed converter is comparable with those of the fast-transient DC-DC converter. The comparison clearly shows the improvements of proposed boost-buck design, which provides one of the fastest transient responses with lower output-voltage ripple.

Meanwhile, this research can be a challenge for future researchers in DC-DC converter field. As shown in Figure 1, the proposed converter uses two switches that work simultaneously. Compared to a conventional converter, this converter may have efficiency issues due to the double switching process. Future research is expected to address the possibility of degradation in the conversion efficiency. In this case, the method of zero-voltage-zero-current switching can be developed to improve conversion efficiency [23][24]. Thus, the proposed boost-buck converter is suitable for practical applications, presenting extremely fast transient response and low output-voltage ripple.

4 Conclusion

The novel cascaded boost-buck converter is proposed to improve the transient response of the DC-DC converter. The converter consists of a cascaded configuration of the boost and buck stages. The boost-stage provides sufficient energy in the shared capacitor to supply the buck-stage by converting the input voltage to the shared capacitor voltage. Meanwhile, the buck-stage converted

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the shared capacitor voltage to the output voltage. By defining the shared capacitor voltage higher than the output voltage, the buck-stage unitizes the energy stored in the shared capacitor to keep the output voltage to be nominal value. The proposed converter uses separate inductors for boost and buck stages. By using a small buck-inductance, the buck-stage allows a rapidly change in the output current. The simulation results show that the recovery time can be improved to 2 μs in the step-up load current change of 1 A with a maximum output voltage ripple of 15 mV. The proposed architecture boost-buck converter achieved the fastest-transient response with low output-voltage ripple and rapidly generated a stable output voltage despite the load current variation.

Acknowledgements

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The Response to **the first** reviewer's comments

1. The 1st comment:

Mention the short specific name of your proposed method or model which give the best solution (performance) of your research in this paper (in abstract and method) because Fast-Transient Response is too general. Ex. Boost-buck architecture.

Response:

Authors would like to thank the reviewer for favorable comments. We have already modified the title by emphasizing the proposed model. The revised title of this manuscript is "A Novel Boost-Buck Converter Architecture for Improving Transient Response and Output-Voltage Ripple". With regard to this modification, the last sentence of the abstract is also modified.

Modification:

Title

Development of Boost-Buck Converter with Fast-Transient Response and Low Output-Voltage Ripple

Abstract (last sentence)

By harnessing the energy stored in the shared capacitor, the transient response can be improved to 2 μs in a step-up load current change of 1 A with an output-voltage ripple of 15 mV.

After the modification:

Title

A Novel Boost-Buck Converter Architecture for Improving Transient Response and Output-Voltage Ripple

Abstract (last sentence)

By harnessing the energy stored in the shared capacitor, the transient response of the boost-buck architecture can be improved to 2 μs in a step-up load current change of 1 A with an output-voltage ripple of 15 mV.

2. The 2nd comment:

Give the specific structure i.e. section 2 method discuss i.e …., section 3 research and discussion discuss i.e….,…….finally condluded in section 4.

Response:

In this regard, we have modified the last paragraph of the introduction by separating it into two parts. In the revised manuscript, the last paragraph of introduction includes the specific discussions of each section.

Modification:

The part of the article before modification:

I. Introduction (Last paragraph)

In this paper, a novel cascaded architecture of boost-buck converter is proposed. Similar architecture had been developed for Wireless Power Transfer System [13] and electric bus charger [14]. In Ref. [13], the architecture is used to perform an optimal impedance matching and dynamic load isolation. Meanwhile, the architecture given in Ref. [14] is utilized to accommodate input and battery voltage. Both applications are not intended to improve the transient response. In this study, the boost-buck architecture for improving transient response is investigated. This includes architecture description and theoretical formulation of the new method as well as working operation principal of the proposed converter. Several cases are

simulated, and the results of the proposed converter are analyzed and compared with those obtained from conventional buck-boost converter.

After the modification:

I. Introduction (Last two paragraphs)

In this paper, a novel cascaded architecture of boost-buck converter is proposed. Similar architecture had been developed for Wireless Power Transfer System [13] and electric bus charger [14]. In Ref. [13], the architecture is used to perform an optimal impedance matching and dynamic load isolation. Meanwhile, the architecture given in Ref. [14] is utilized to accommodate input and battery voltage. Both applications are not intended to improve the transient response.

In this study, the boost-buck architecture for improving transient response is investigated. This manuscript is divided into four sections. Section 1 presents the background and overview of the proposed method. In Section 2, the architecture description and theoretical formulation of the new method as well as the working operation principal of the proposed converter are discussed. Several important cases are simulated in Section 3. The experimental results are subsequently analyzed and compared with those obtained by similar experiments on conventional buck-boost converters. Finally, conclusions are drawn in Section 4.

3. The 3rd comment:

Enlarge both figures by converting them from landscape to portrait model in order can be seen by the reader.

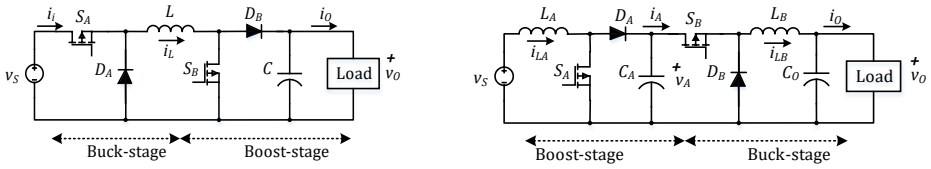
Response:

We have converted and enlarged Figures 1 - 4 from landscape into a portrait model.

Modification:

The part of the article before modification:

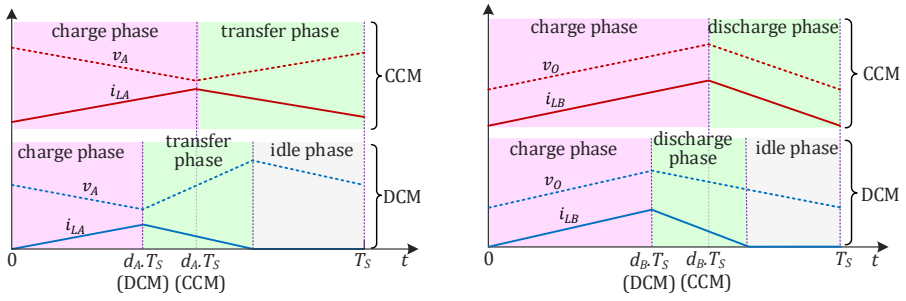
Figure 1:



(a) a non-inverting buck-boost converter (b) the proposed boost-buck converter

Figure 1 A non-inverting buck-boost converter and the proposed boost-buck converter

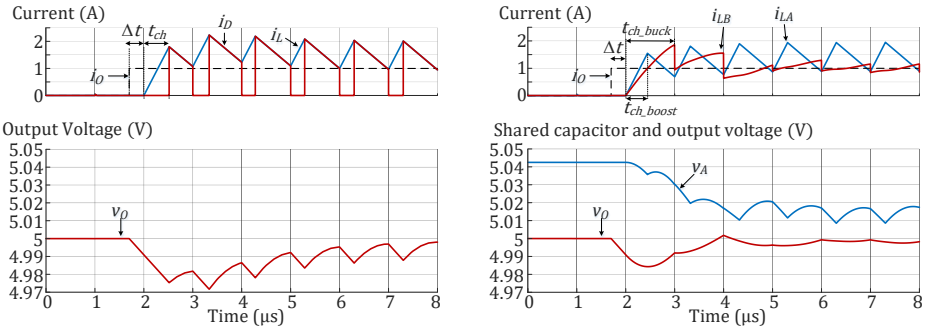
Figure 2:



(a) boost-stage (b) buck-stage

Figure 2. Key waveform of the boost and buck stages

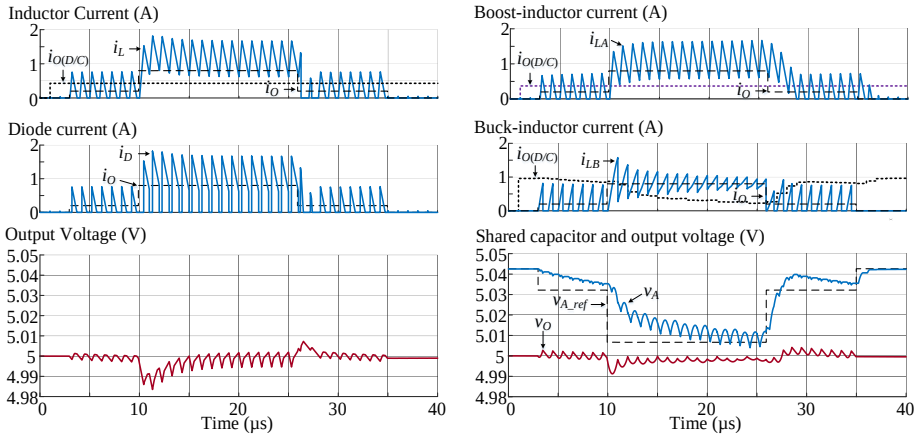
Figure 3:



(a) in buck-boost converter (b) in boost-buck converter

Figure 3 Simulated current and voltage when load current is applied

Figure 4:

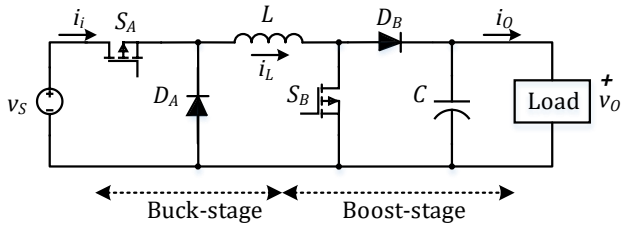


(a) in buck-boost converter (b) in the proposed boost-buck converter

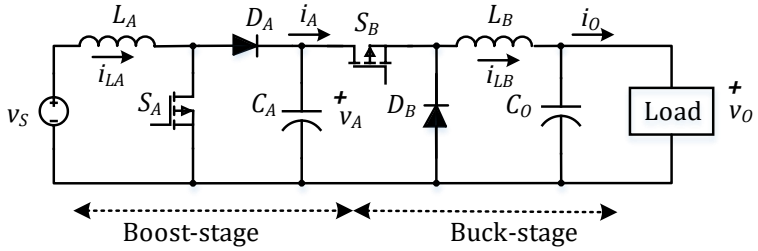
Figure 4 Simulated waveforms for current, voltage and duty cycle

After the modification:

Figure 1:



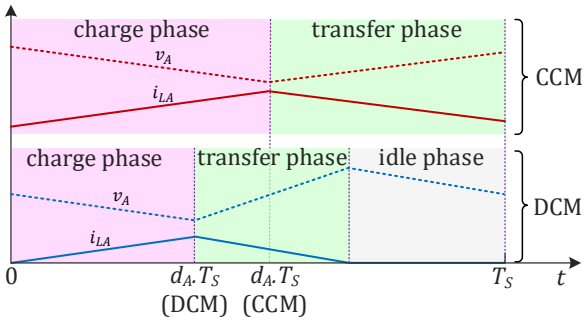
(a) a non-inverting buck-boost converter



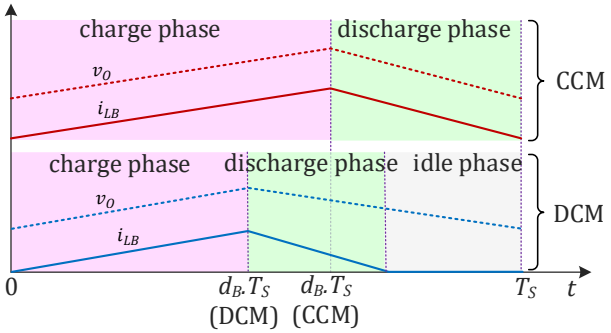
(b) the proposed boost-buck converter

Figure 1 A non-inverting buck-boost converter and the proposed boost-buck converter

Figure 2:



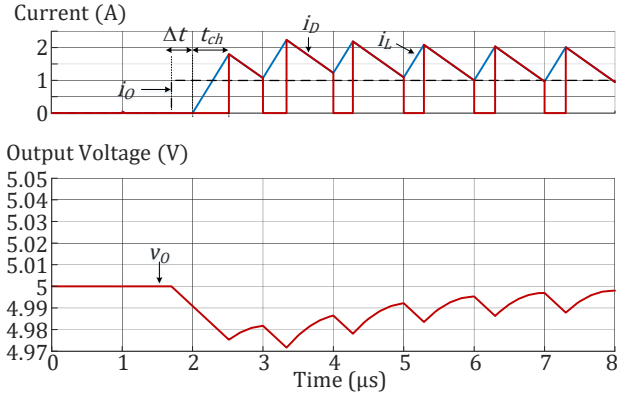
(a) boost-stage



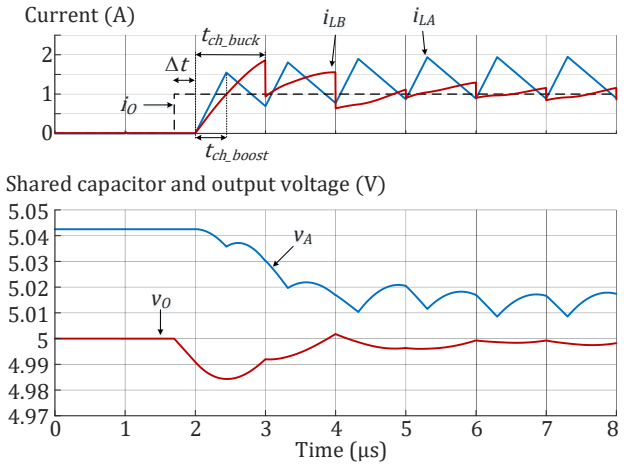
(b) buck-stage

Figure 2 Key waveform of the boost and buck stages

Figure 3:



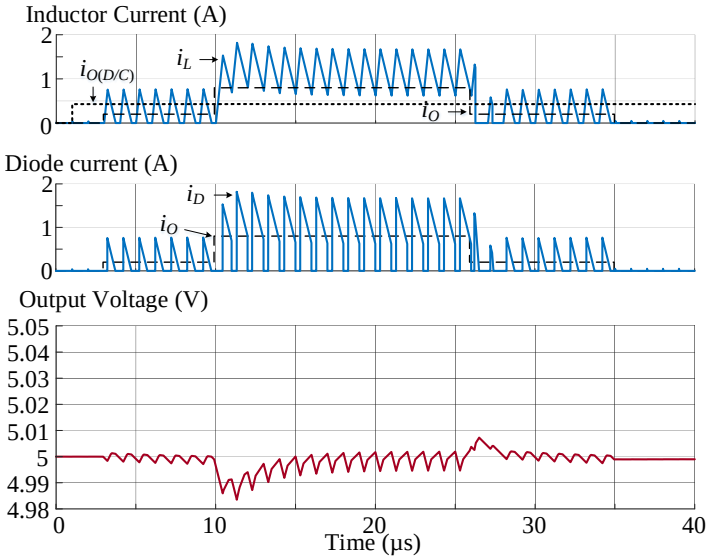
(a) in buck-boost converter



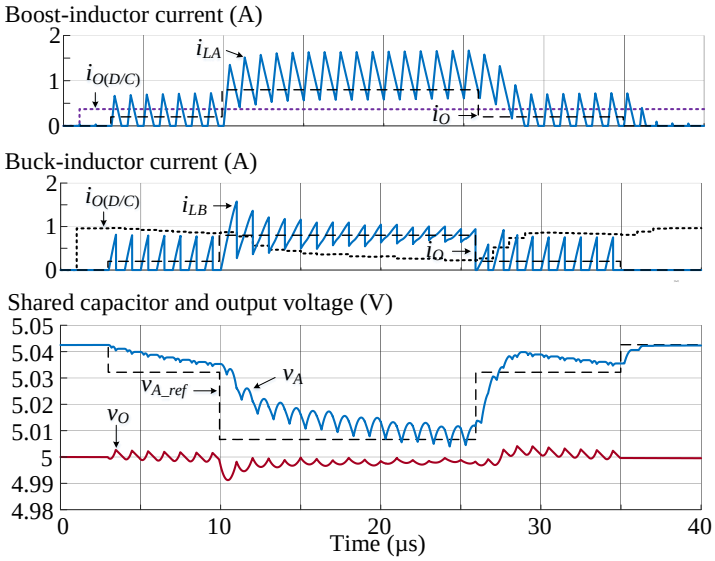
(b) in boost-buck converter

Figure 3 Simulated current and voltage when load current is applied

Figure 4:



(a) in buck-boost converter



(b) in the proposed boost-buck converter

Figure 4 Simulated waveforms for current, voltage and duty cycle

4. The 4th comment:

Enlarge this figure (Figure 5).

Response:

We have enlarged Figure 5.

Modification:

The part of the article before modification:

Figure 5

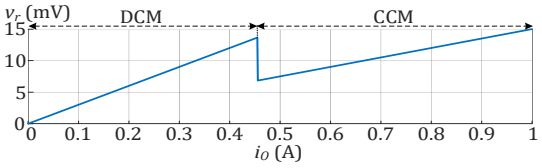


Figure 5 The output-voltage ripple as the output current

After the modification:

Figure 5

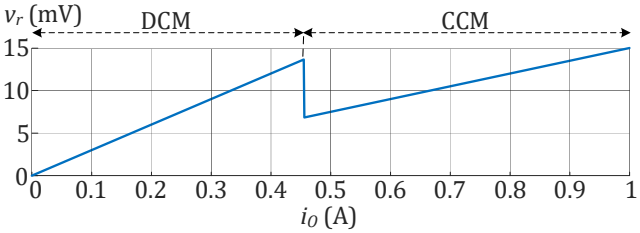


Figure 5 The output-voltage ripple as the output current

5. The 5th comment:

What is the weakness of your paper? Please describes the example solution as the future works to overcome this problem (This comment refers to the last sentence of conclusion).

Response:

- For sake of modification, the last paragraph of the section of Results and Discussion is divided into two separated paragraphs. Additional comments regarding the future works are inserted before the last sentence of the last paragraph within this section.

Modification:

The part of the article before modification:

3. Results and Discussions (the last paragraph)

Table 2 summarizes the measured characteristic of the published DC-DC converter. Using a 1 MHz switching frequency, a pseudo-current dynamic acceleration in Ref. [12] can be utilized to improve the transient response to 2 µs. However, the proposed boost-buck converter performs a better output voltage quality due to its lower output-voltage ripple. Therefore, the performance of the proposed converter is comparable with those of the fast-transient DC-DC converter. The comparison clearly shows the improvements of proposed boost-buck design, which provides one of the fastest transient responses with lower output-voltage ripple.

After the modification:

3. Results and Discussions (the last two paragraphs)

Table 2 summarizes the measured characteristic of the published DC-DC converter. Using a 1 MHz switching frequency, a pseudo-current dynamic acceleration in Ref. [12] can be utilized to improve the transient response to 2 µs. However, the proposed boost-buck converter performs a better output voltage quality due to its lower output-voltage ripple. Therefore, the performance of the proposed converter is comparable with those of the fast-transient DC-DC converter. The comparison clearly shows the improvements of proposed boost-buck design, which provides one of the fastest transient responses with lower output-voltage ripple.

Meanwhile, this research can be a challenge for future researchers in DC-DC converter field. As shown in Figure 1, the proposed converter uses two switches that work simultaneously. Compared to a conventional converter, this converter may have efficiency issues due to the double switching process. Future research is expected to address the possibility of degradation in the conversion efficiency. In this case, the method of zero-voltage-zero-current switching can be developed to improve conversion efficiency [23][24]. Thus, the proposed boost-buck converter is suitable for practical applications, presenting extremely fast transient response and low output-voltage ripple.

- In the revised manuscript, we also added two references (i.e. Refs. [23] and [24]).

After the modification:

References

[23] R.H. Ashique and Z. Salam, *A Family of True Zero Voltage Zero Current Switching (ZVZCS) Nonisolated Bidirectional DC–DC Converter with Wide Soft Switching Range*, IEEE Trans. on Industrial Electronics, **64**(7), pp. 5416-27, 2017.

[24] Y. Zhang, XF. Cheng and C. Yin, *A Soft-Switching Non-Inverting Buck–Boost Converter With Efficiency and Performance Improvement*, IEEE Trans. on Power Electronics, **34**(12), pp. 11526-30, 2019.

6. The 6th comment:

If you get a grant to finance this research, please complete it with the contract number.

Response:

We have added the contract number of the grant.

Modification:

The part of the article before modification:

Acknowledgements

The research is supported by Sekolah Tinggi Teknologi Adisutjipto under the grant of Strategic Research.

After the modification:

Acknowledgements

The research is supported by Sekolah Tinggi Teknologi Adisutjipto under the grant of Strategic Research No. 026/K2.1/P3M/V/2019.

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3. Does the abstract reflect the paper content?	☑	☐	☐
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6. Do the data presentation and interpretation valid and reasonable?	☑	☐	☐
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	Very good	Good	Fair	Poor
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Signature of reviewer:

Surabaya, 21 Nopember 2020

(Dr. Amirullah, ST, MT)

D. Note from the editors

A Novel Boost-Buck Converter Architecture for Improving Transient Response and Output-Voltage Ripple

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Abstract. Buck-boost converters are widely used in the development of DC-DC converters. Several techniques and algorithms have been introduced to improve the transient response of buck-boost converters. However, due to the opposite trends of the output current change and the output voltage change, undershoot or overshoot in the output voltage still seems to be inevitable. In order to overcome this problem, a novel boost-buck converter architecture is proposed to build a fast transient response DC-DC converter. The converter consists of a cascaded configuration of the boost and buck stages. The boost stage converts the input voltage to the shared capacitor voltage and the buck stage supplies energy to the load by converting the shared capacitor voltage to the output voltage. By harnessing the energy stored in the shared capacitor, the transient response of the boost buck converter can be improved to 2 μs in a step-up load current change of 1 A with an output-voltage ripple of 15 mV.

Keywords: *DC-DC converter; boost; buck; fast-transient; low-ripple.*

1 Introduction

DC-DC converters are widely used in power management technology for the development of modern integrated circuits and systems. The widespread use of portable devices (e.g. digital cameras, cellular phones and tablet computers) require a high-performance DC-DC converter for ensuring the quality of the power supply. In battery-powered systems, a fully charged battery usually possesses a higher voltage than its nominal voltage, while a discharged battery has a lower one. In order to generate a stable power supply voltage a buck-boost converter is generally used because of its wide input voltage range [1-3]. Moreover, a stable voltage is required in high-performance systems to cope with the dynamically varying workload, especially in modern microprocessor systems. When the system switches between idle mode and active mode there is a large

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difference in the required current load. Meanwhile, in active mode the processor usually has varying load. Unfortunately, the output current slew rate of the buck-boost converter is usually limited by the inductor. Thus, the supply voltage fed by the converter will encounter undershoot or overshoot and deviate from its nominal value. Overshoot may cause a raise in chip temperature, while undershoot may force the processor to insert 'idle' instructions to reduce the load current. Furthermore, the processor may fail to execute any instructions or dismiss some data [4,5]. The aforementioned facts show that the slew rate limitation in the output current must be mitigated and a fast-transient response is an important design consideration in developing a DC-DC converter.

In a buck-boost converter, the incapability of the inductor to suddenly change the current will violate the output voltage range. It will take some time to return the output voltage to its nominal value, resulting in undershoot or overshoot in the output voltage. Furthermore, when the converter works in boost mode it suffers from output current change due to the opposite trends of the output-current change and the output-voltage change.

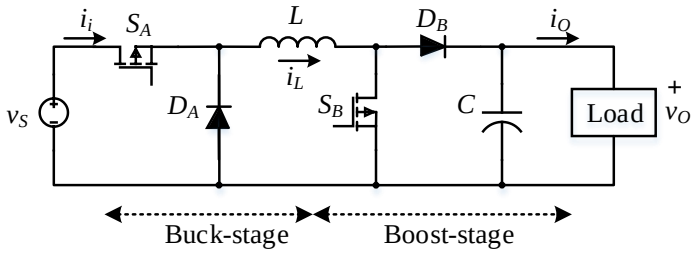
Several methods and algorithms have been developed to alleviate undershoot and overshoot in the output voltage of buck-boost converters [6-12]. In [6], adaptive pulse skipping and adaptive compensation capacitance techniques were used to reduce the transient response to 59 µs in a 400 mA load. The converter was reported to be able to achieve a fastest transient response of 45 µs under a load current of 200 mA using a hybrid buck-boost feed-forward technique [7]. In general, the transient response can be reduced by using a higher switching frequency. Using a switching frequency higher than 1 MHz may reduce the transient response to under 20 µs [8-12]. In [8], a switching frequency of 3 MHz could support on-duty modulation to achieve a fast line transient response of 17.2 µs at a load change from 10 to 600 mA. Meanwhile, in [11], by utilizing a load-dependent on/off time, the transient response could be improved to 10 µs at a 600 mA load current. Utilization of a higher switching frequency may improve the transient response, but it produces higher switching loss and circuit diagram complexity. The aforementioned studies [8-12] could enhance the quality of the transient response, but undershoot and overshoot in the output voltage were still inevitable. Thus, the development of a new method to support a fast transient response DC-DC converter is of interest.

In this paper, a novel cascaded boost-buck converter architecture is proposed. A similar architecture has been developed for a wireless power transfer system [13] and an electric bus charger [14]. In [13], this architecture was used to perform optimal impedance matching and dynamic load isolation. Meanwhile, the architecture described in [14] was utilized to accommodate the input and battery voltage. However, neither application intended to improve the transient response.

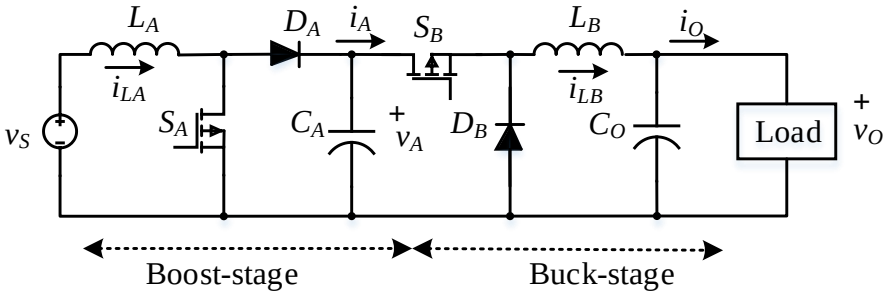
This manuscript is divided into four sections. Section 1 presents the background and an overview of the proposed method. In Section 2, a description of the architecture and the theoretical formulation of the new method as well as the working principle of the proposed converter are discussed. Several relevant simulated cases are presented in Section 3. The experimental results are subsequently analyzed and compared with those obtained in similar experiments on conventional buck-boost converters. Finally, the conclusions are drawn in Section 4.

2 Research Method

Figure 1(a) shows a buck-boost converter that is widely used, while Figure 1(b) shows the proposed boost-buck converter. They both have lower voltage stress on the components due to a non-inverting output voltage [15-17]. The proposed boost-buck converter is a development of the one reported in [18]. It uses separate inductors for the boost stage and the buck stage. An additional shared capacitor C_A filters the boost-stage output voltage and constitutes the voltage source for the buck stage.



(a) A non-inverting buck-boost converter



(b) The proposed boost-buck converter

Figure 1 A non-inverting buck-boost converter and the proposed boost-buck converter.

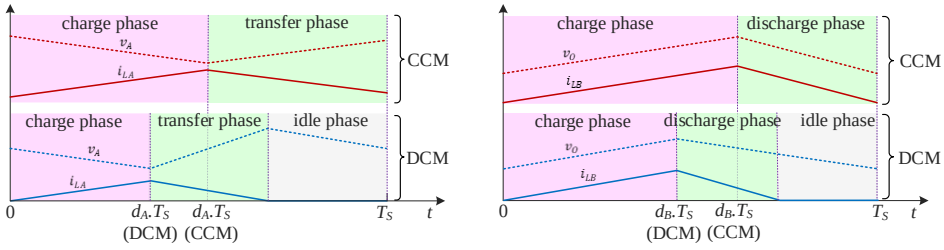
2.1 The Boost-stage

In the proposed boost-buck converter, the boost stage steps up the input voltage, v_s, to the shared capacitor voltage, v_A. Figure 2(a) shows the key waveform when the boost stage operates in discontinuous-current mode (DCM) and continuous-current mode (CCM) with switching period T_S and duty cycle d_A. When the stage works in DCM, three unique phases appear during each switching period: the charge, transfer, and idle phases [11]. During the charge phase, the power switch S_A is on, thus the voltage source v_S energizes the boost-inductor L_A, while the buck stage is energized by the energy stored in the shared capacitor. Meanwhile, in the transfer phase, the power switch S_A is turned off and the energy stored in the boost-inductor is released and becomes boost-stage output current i_A. When the stored energy in the boost inductor has run out, the stage falls into the idle phase. By applying KVL and KCL the state space representation for the charge phase can be expressed as follows:

$$\begin{bmatrix} \frac{di_{LA}(t)}{dt} \\ \frac{dv_A(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{C_A R_L} \end{bmatrix} \begin{bmatrix} i_{LA}(t) \\ v_A(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_A} \\ 0 \end{bmatrix} v_S \tag{1}$$

Meanwhile, the state space representation for the transfer phase and the idle phase can be formulated as follows:

$$\begin{bmatrix} \frac{di_{LA}(t)}{dt} \\ \frac{dv_A(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_A} \\ \frac{1}{C_A} & -\frac{1}{C_A R_L} \end{bmatrix} \begin{bmatrix} i_{LA}(t) \\ v_A(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_A} \\ 0 \end{bmatrix} v_S \tag{2}$$



(a) Boost-stage (b) Buck-stage

Figure 2 Key wave forms of the boost and buck stages.

When there is no net change in the output current and voltage during a switching period, the stage reaches steady state. From the Eqs. (1) and (2), the output current i_A in DCM can be expressed as follows:

$$i_A = \frac{{v_S}^2 {d_A}^2 T_S}{2(v_A - v_S)L_A} \tag{3}$$

Therefore, boost-stage duty cycle d_A may track boost-stage output current i_A as:

$$d_A = \sqrt{\frac{2i_A(v_A - v_S)L_A}{{v_S}^2 T_S}} \tag{4}$$

when the stage works in CCM, only two unique phases appear: the charge phase and the transfer phase. The changes of output current Δi_A and output voltage Δv_A within one switching period T_S can be derived as:

$$\Delta i_A = \frac{T_S}{L_A}(v_S - v_A + d_A v_A) \tag{5}$$

$$\Delta v_A = \frac{T_S}{C_A}(i_{LA}(1 - d_A) - i_A) \tag{6}$$

The stage reacts to output current change i_A by determining a new duty cycle d_A in order to change i_{LA}:

$$d_A = \frac{\Delta i_A v_A L_A + (v_A - v_S)v_S T_S}{v_S v_A T_S} \tag{7}$$

The output current condition where the boost stage is at the boundary between DCM and CCM is:

$$i_{O(D/C)} = \frac{(v_A - v_S){v_S}^2 T_S}{2{v_A}^2 L_A} \tag{8}$$

The relationship between the changes of output current Δi_A and voltage Δv_A can be derived as:

$$\Delta v_A = -\frac{\Delta i_A i_A v_A L_A}{{v_S}^2 C_A} \tag{9}$$

Eq. (9) clearly states an opposite trend between both parameters. This essential problem implies that the output current increases cause the output voltage to drop and vice versa. This induces an output voltage range violation in the buck-boost converter due to the stage directly supplying energy to the load. Therefore, the stability of the output voltage suffers from an output current change when the buck-boost converter works in boost mode. Although it is possible to alleviate this problem, it will be still inevitable in the transient stage and produce overshoot or undershoot in the output voltage.

2.2 The Buck Stage

The buck stage steps down the shared capacitor voltage, v_A, to the output voltage, v_O. Figure 2(b) shows the key waveform when the buck stage operates in DCM and CCM with switching period T_S and duty cycle d_B. When the stage works in

DCM, three unique phases appear in each switching period: the charge, discharge, and idle phases [11]. During the charge phase, the power switch S_B is on and thus the voltage source v_S energizes the inductor L_B. Meanwhile during the discharge phase, the power switch S_B is turned off and the energy stored in the buck inductor is released to the output capacitor and supplies the load. When there is no more energy stored in the buck inductor, the stage falls into the idle phase. By applying KVL and KCL, the state space representation for the charge phase can be expressed as follows:

$$\begin{bmatrix} \frac{di_{LB}(t)}{dt} \\ \frac{dv_O(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_B} \\ \frac{1}{C_O} & -\frac{1}{C_O R_L} \end{bmatrix} \begin{bmatrix} i_{LB}(t) \\ v_O(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_B} \\ 0 \end{bmatrix} v_A \tag{10}$$

Meanwhile, the state space representation for the discharge and idle phases can be formulated as:

$$\begin{bmatrix} \frac{di_{LB}(t)}{dt} \\ \frac{dv_O(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_B} \\ \frac{1}{C_O} & -\frac{1}{C_O R_L} \end{bmatrix} \begin{bmatrix} i_{LB}(t) \\ v_O(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_A \tag{11}$$

When the stage reaches steady state the output current in DCM can be calculated as:

$$i_O = \frac{v_A - v_O}{2L_B} {d_B}^2 T_S \left(1 + \frac{v_A - v_O}{v_O}\right) \tag{12}$$

Therefore, buck-stage duty cycle d_B may track output current i_O as follows:

$$d_B = \sqrt{\frac{2i_O L_B v_O}{v_A(v_A - v_O)T_S}} \tag{13}$$

Meanwhile, when the buck stage works in CCM only two unique phases appear: charge and discharge. By using Eqs. (10) and (11), the changes of buck-inductor current Δi_{LB} and output voltage Δv_O within one switching period T_S can be derived as Eqs. (14) and (15) respectively:

$$\Delta i_{LB} = \frac{T_S}{L_B}(v_A d_B - v_O) \tag{14}$$

$$\Delta v_O = \frac{T_S}{C_O}(i_{LB} - i_O) \tag{15}$$

In this mode, the stage reacts to output current changes Δi_O by determining a new duty cycle in order to change i_{LB}. From Eq. (14), duty cycle d_B can be calculated as:

$$d_B = \frac{\Delta i_O L_B + v_O T_S}{T_S v_A} \tag{16}$$

The output current condition where the buck stage is at the boundary between DCM and CCM is:

$$i_{O(D/C)} = \frac{v_A v_O - {v_O}^2}{2 L_B v_A} T_S \tag{17}$$

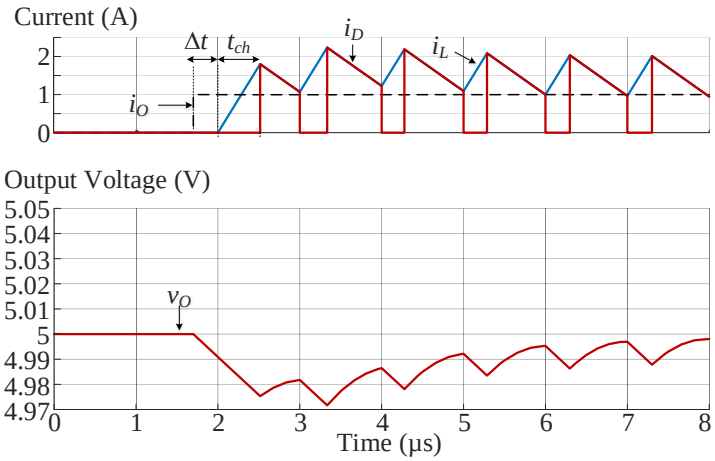
2.3 Working Principle of the Boost-Buck Converter

The stability of the output voltage in the buck-boost converter suffers from an output current change when it works in the boost-stage CCM. The upper part of Figure 3(a) shows an example of the waveforms of inductor current i_L (blue line), diode current i_D (red) and load current i_O (black-dashed). As a load current of 1 A is applied at t = 1.7 µs, the boost stage reacts by increasing its duty cycle to prolong the charge phase in order to increase the inductor current. However, during this phase no energy is transferred from the inductor to the load. This causes a voltage drop in transient period $\Delta t + t_{ch}$. The deleterious effect of an output current change is clearly illustrated by the output voltage curve in the lower part of Figure 3(a).

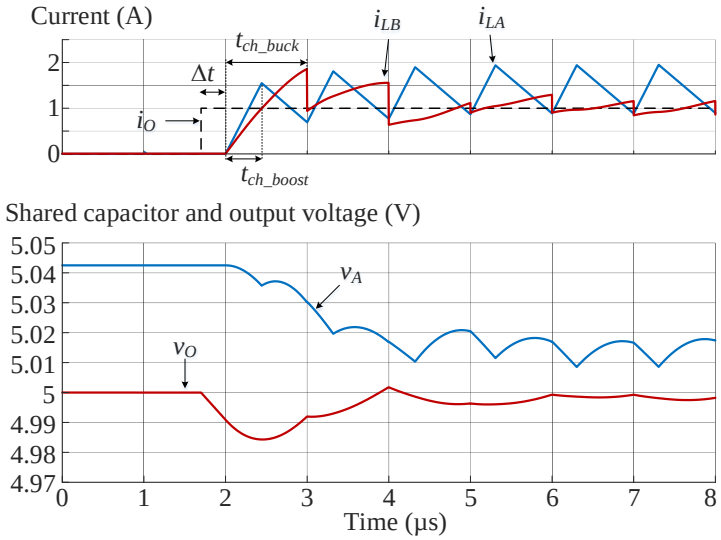
A simplified qualitative way to visualize the different basic operations of the proposed boost-buck converter and a conventional buck-boost converter is to consider the use of the shared capacitor as a temporary energy-storing element. The energy stored in the shared capacitor can be used to maintain the output voltage at the nominal value if its voltage v_A is higher than the output voltage v_O. Such energy can be defined as $E_A = \frac{1}{2} C_A ({v_A}^2 - {v_O}^2)$, so that the shared capacitor voltage that must be available when the converter is drawn by a load current of i_O can be derived as follows:

$$v_A = \sqrt{\frac{2(i_{O(max)} - i_O) v_O {v_S}^2 T_S + 2(i_{O(max)} - i_O)^2 {v_O}^2 L_A}{C_A {v_S}^2} + {v_O}^2} \tag{18}$$

The actual shared capacitor voltage may not be equal to v_A as calculated in Eq. (18). In the foregoing analysis, v_{A_ref} defines the result of Eq. (18) and v_A is the actual shared capacitor voltage. To recover the energy balance after an output current change, PID compensation is adopted to return v_A back to v_{Aref} by slightly increasing or decreasing the duty cycle for a period of time.



(a) In the buck-boost converter



(b) In the boost-buck converter

Figure 3 Simulated current and voltage when a load current is applied.

3 Results and Discussions

The proposed boost-buck DC-DC converter is designed to achieve a faster transient response with smaller output-voltage ripple. Several simulations utilizing the system parameters listed in Table 1 were conducted to investigate the performance of the proposed converter. For the sake of verification of the

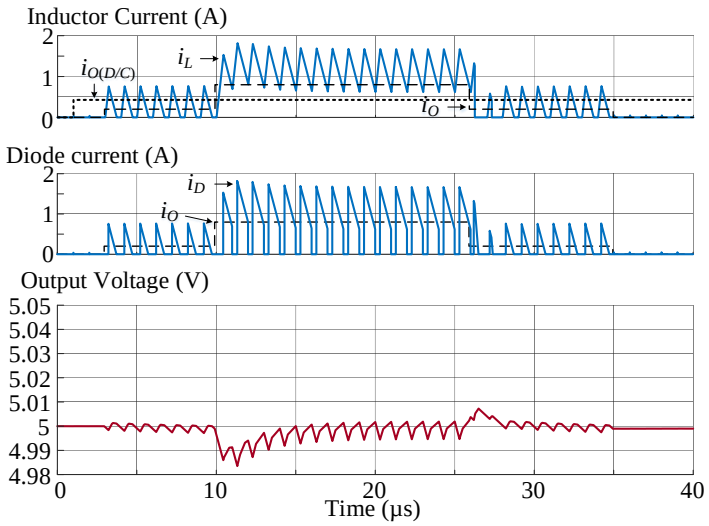
obtained transient response, load current changes were applied to the converter for a short time period.

Table 1 Parameters of proposed boost-buck converter.

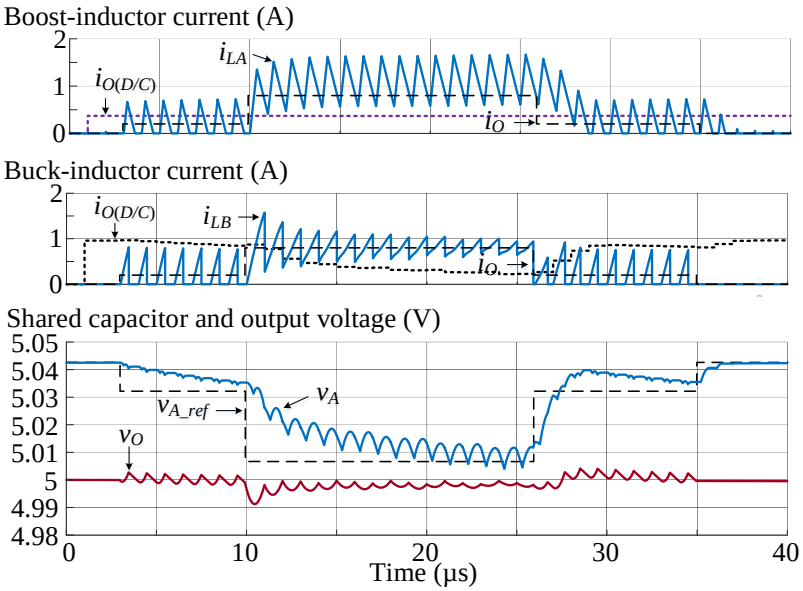
Parameters	Symbols	Values
Input voltage	v_S	3.5 V
Output voltage	v_O	5 V
Boost-inductance	L_A	1 µH
Buck-inductance	L_B	22 nH
Shared capacitor	C_A	33 µF
Output capacitor	C_O	33 µF
Maximum output current	i_O(max))	1 A
Switching frequency	f_S	1 MHz

Figure 4 presents a comparison of the simulated transient waveform for current and voltage between a conventional buck-boost converter and the proposed boost-buck converter. In this simulation, an initial step-up load current of 0.2 A was applied at t = 2.8 µs. Owing to the fact that i_O was lower than $i_{O(D/C)}$, the operation mode was set to DCM and a new duty cycle was determined. In the proposed boost-buck converter, the increased duty cycle yields an increase of boost-inductor current i_{LA} and buck-inductor current i_{LB}. Regarding the output voltage, as stated in Eqs. (4) and (13), the duty cycle of the boost and buck stages of both converters have the same trends as their output voltage, therefore overshoot and undershoot do not occur.

When a load change of 0.6 A was applied at t = 9.8 µs, i_O was higher than $i_{O(D/C)}$. Thus, the converter increased the duty cycle and switched the operation to CCM. In a buck-boost converter, an increase of the boost-stage duty cycle introduces an output voltage drop. In the proposed converter, however, an increase of the boost-stage duty cycle results in a decrease of shared capacitor voltage v_A only. In spite of this, as long as v_A is greater than v_O, the output voltage can be properly kept constant by the buck stage. By comparing the output current injected into the output capacitor it can be seen that the diode current, i_D, in the buck-boost converter is discontinuous or pulsating, while the buck-inductor current, i_{LB}, in the proposed converter is a sawtooth. These phenomena ensure that the output-voltage ripple of the proposed converter is lower than that of a conventional buck-boost converter.



(a) In the buck-boost converter



(b) In the proposed boost-buck converter

Figure 4 Simulated waveforms for current, voltage and duty cycle.

As stated in Eq. (16), the duty cycle of the boost-stage CCM depends on output-current change Δi_O and the DC level of the input voltage v_S and output voltage v_O. When a conventional buck-boost converter is in the boost stage, the converter

reacts to a change in the duty cycle according to Δi_O only because of the fixed values of v_S and v_O. Therefore, in the case of a light to heavy load change, the duty cycle is raised for certain switching periods and returned back to the steady-state value afterwards. Meanwhile, in the proposed converter, the boost-stage determines the duty cycle according to Δi_O and shared-capacitor voltage v_A. Due to the opposite reaction between both parameters, the variation of boost-stage duty cycle d_A in the proposed converter is smaller than in a conventional converter. The same trend also occurs to boost-inductor current i_{LA}. This makes the boost stage of the proposed converter seem to have a more sluggish response than that of a conventional one.

As the load becomes lower, the converter determines a lower duty cycle to decrease the inductor current. In a buck-boost converter, a lower boost-stage duty cycle results in a decrease of the charge phase while increasing the transfer phase. More time for the transfer phase increases i_D and causes an upward violation of the output voltage range. Meanwhile, in the proposed converter more time for the transfer phase increases boost-stage output current i_A and shared capacitor voltage v_A. However, a decrease in output load current i_O will be followed by an increase in v_{A_ref}, as shown by Eq. (18). Consequently, v_A will be able to reach v_{A_ref} faster.

In the proposed converter, when the output current changes, the buck-stage determines the corresponding adjustment amount of the duty cycle according to Eqs. (13) or (16) to change the buck-inductor current in order to keep the output voltage constant at its nominal value. Due to the inductor's tendency to resist changes in current, the output current slew rate is fundamentally limited due to the presence of the buck inductor. To allow more rapid changes in the buck-inductor current, the level of inductance may be reduced. This can be done because the proposed architecture uses separate inductors for the boost and buck stages. In contrast with a conventional buck-boost converter, which uses the same inductor for both stages, reducing the inductance may improve the transient response, but it will increase the output-voltage ripple when it is in the boost stage.

The level of buck inductance must be carefully determined. Using a smaller buck inductance will reduce $i_{O(D/C)}$ and thus may force the buck stage to work in DCM for more cases and increase the output-voltage ripple. The proposed converter uses a buck inductance of 22 nH. By harnessing the energy stored in the shared capacitor, the buck stage allows the current to flow through the buck inductor with a rate of change up to 1.91 A/μs when the maximum load current is applied after no-load condition. Therefore, this stage is able to recover the output voltage to 2 μs. By comparing the transient response time and output-voltage ripple

between a conventional buck-boost converter and the proposed converter in Figure 3 and Figure 4 it is clear that the transient response time of the proposed converter is shorter than that of a conventional one. Moreover, to further enhance the transient response and efficiency, several methods have been introduced to further develop the proposed converter [19]-[22].

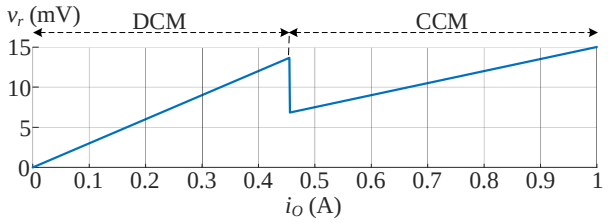


Figure 5 The output-voltage ripple as the output current.

The proposed converter may provide a better output-voltage ripple v_r when drawn by a large output current and the buck stage works in CCM. In this case, buck-stage duty cycle d_B approaches one, thus C_A, L_B, and C_O constitute a second-order filter. Hence, the output-voltage ripple can be effectively diminished. Figure 5 shows the output-voltage ripple as the output current. The maximum value of the output-voltage ripple is 13.6 mV when the buck stage works in DCM and 15 mV when it works in CCM.

Table 2 summarizes the measured characteristics of the published DC-DC converter. Using a switching frequency of 1 MHz, the pseudo-current dynamic acceleration from [12] can be utilized to improve the transient response to 2 µs. However, the proposed boost-buck converter provides a better output voltage quality due to its lower output-voltage ripple. Therefore, the performance of the proposed converter is comparable with that of a fast-transient DC-DC converter. The comparison clearly shows the improvements of the proposed boost-buck design, which provides one of the fastest transient responses with lower output-voltage ripple.

This research may challenge future researchers in the DC-DC converter field. As shown in Figure 1, the proposed converter uses two switches that work simultaneously. Compared to a conventional converter, this converter may have efficiency issues due to the double switching process. Future research is expected to address the possibility of degradation of the conversion efficiency. In this case, the method of zero-voltage zero-current switching can be developed to improve the conversion efficiency [23,24]. Thus, the proposed boost-buck converter is suitable for practical applications, presenting an extremely fast transient response and low output-voltage ripple.

Table 2 Performance comparison of recent techniques developed in DC-DC converter.

Technique	v_S and v_O	$i_{O(max)}$	f_S	$v_{r(max)}$	$t_{r(min)}$	L/C
Adaptive pulse skipping and compensation capacitance [6]	2.7~4.5 V 3 V	900 mA	1 MHz	N/A	59 µs @400 mA	2.2 µH/20 µF
Hybrid buck-boost feedforward [7]	2.7~4.5 V 3.3 V	500 mA	700 kHz	> 200 mV	45 µs @200 mA	4.7 µH/47 µF
Direct path skipping and on-duty modulation [8]	3.0 V 2.8~5.5 V	1 A	3 MHz	88.3 mV	17.2 µs @600 mA	2.2 µH/33 µF
Hysteretic-current-mode [9]	2.5~5 V 3.3 V	400 mA	≤1.66 MHz	15 mV	15 µs @290 mA	1 µH/10 µF
Power-tracking with fast dynamic voltage scaling [10]	2.5~4.5 V 2~4 V	400 mA	5 MHz	> 175 mV	15 µs @300 mA	1 µH/0.88 µF
Load-dependent on/off time [11]	3.3 V 1.8~5.0V	800 mA	3.3 MHz	90 mV	10 µs @600 mA	1.5 µH/10 µF
Pseudo-current dynamic acceleration [12]	3.3 V 1V~4.5V	200 mA	1 MHz	80 mV	2 µs @200 mA	22 µH/10 µF
Boost-buck architecture (simulated in this work)	3.5~6 V 5 V	1 A	1 MHz	15 mV	2 µs @1 A	1+0.022 µH/ 33+33 µF

v_S/v_O = input/output voltage
$i_{O(max)}$ = maximum load current
f_S = switching frequency
$v_{r(max)}$ = maximum output-voltage ripple
$t_{r(min)}$ = minimum transient response time
L/C = capacitance and inductance used

4 Conclusion

A novel cascaded boost-buck converter architecture was proposed to improve the transient response of the DC-DC converter. The converter consists of a cascaded configuration of the boost and buck stages. The boost stage provides sufficient energy in a shared capacitor to supply the buck stage by converting the input voltage to the shared capacitor voltage. Meanwhile, the buck stage converts the shared capacitor voltage to the output voltage. By defining the shared capacitor voltage higher than the output voltage, the buck stage unitizes the energy stored

in the shared capacitor to keep the output voltage at its nominal value. The proposed converter uses separate inductors for the boost and buck stages. By using a low buck inductance, the buck stage allows rapid changes in the output current. The simulation results showed that the recovery time can be improved to 2 μs with a step-up load current change of 1 A with a maximum output-voltage ripple of 15 mV. The proposed boost-buck converter achieves a fast transient response with low output-voltage ripple and rapidly generates a stable output voltage despite load current variation.

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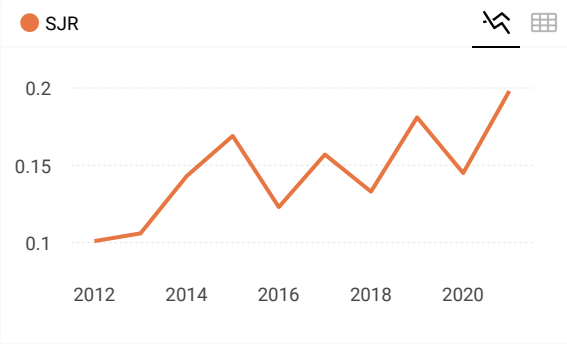

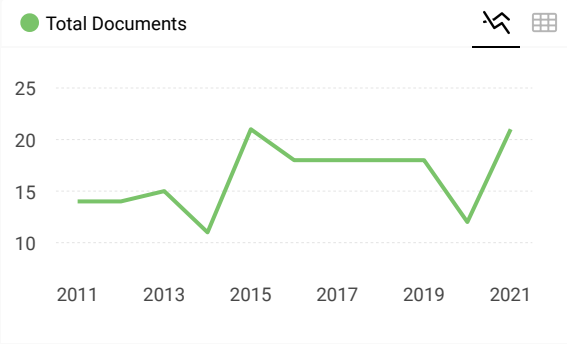

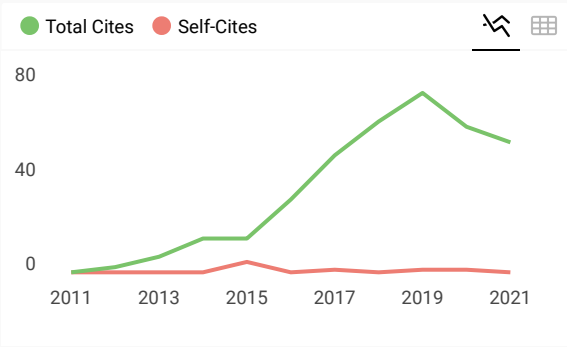

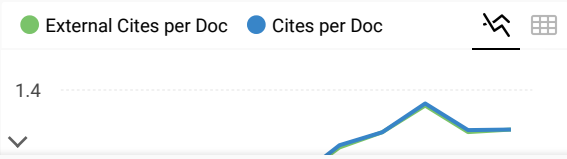

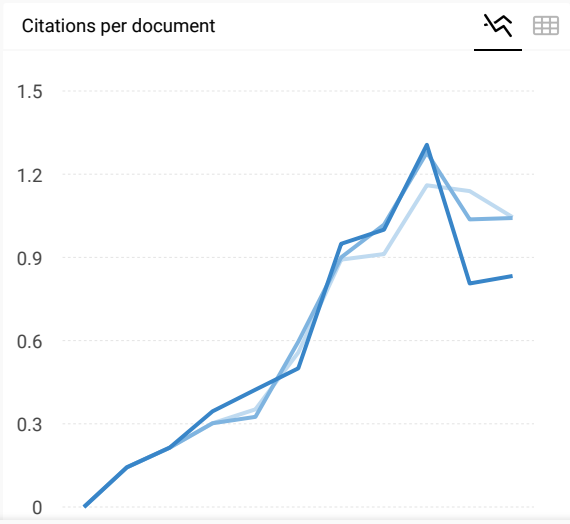

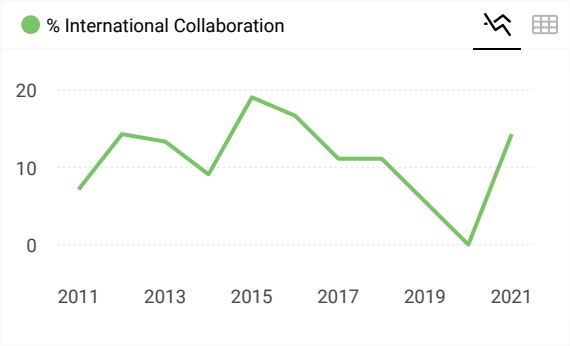

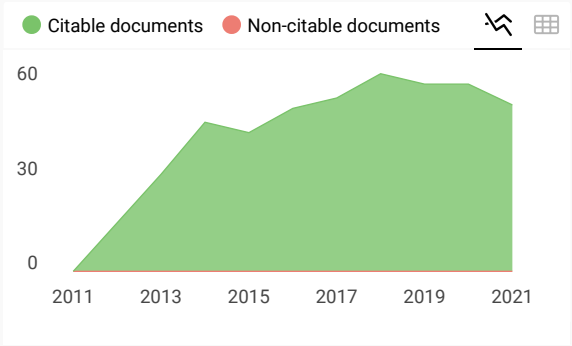

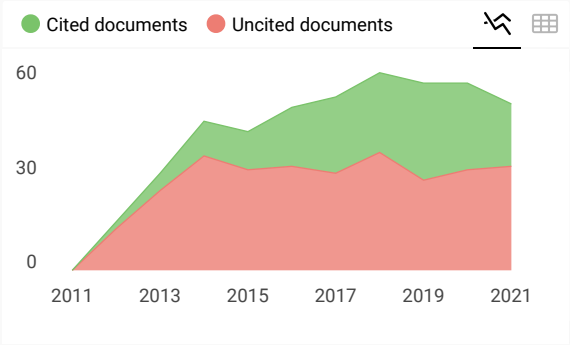

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